COMP 122

Rev 4-13-21

Micro-Programming

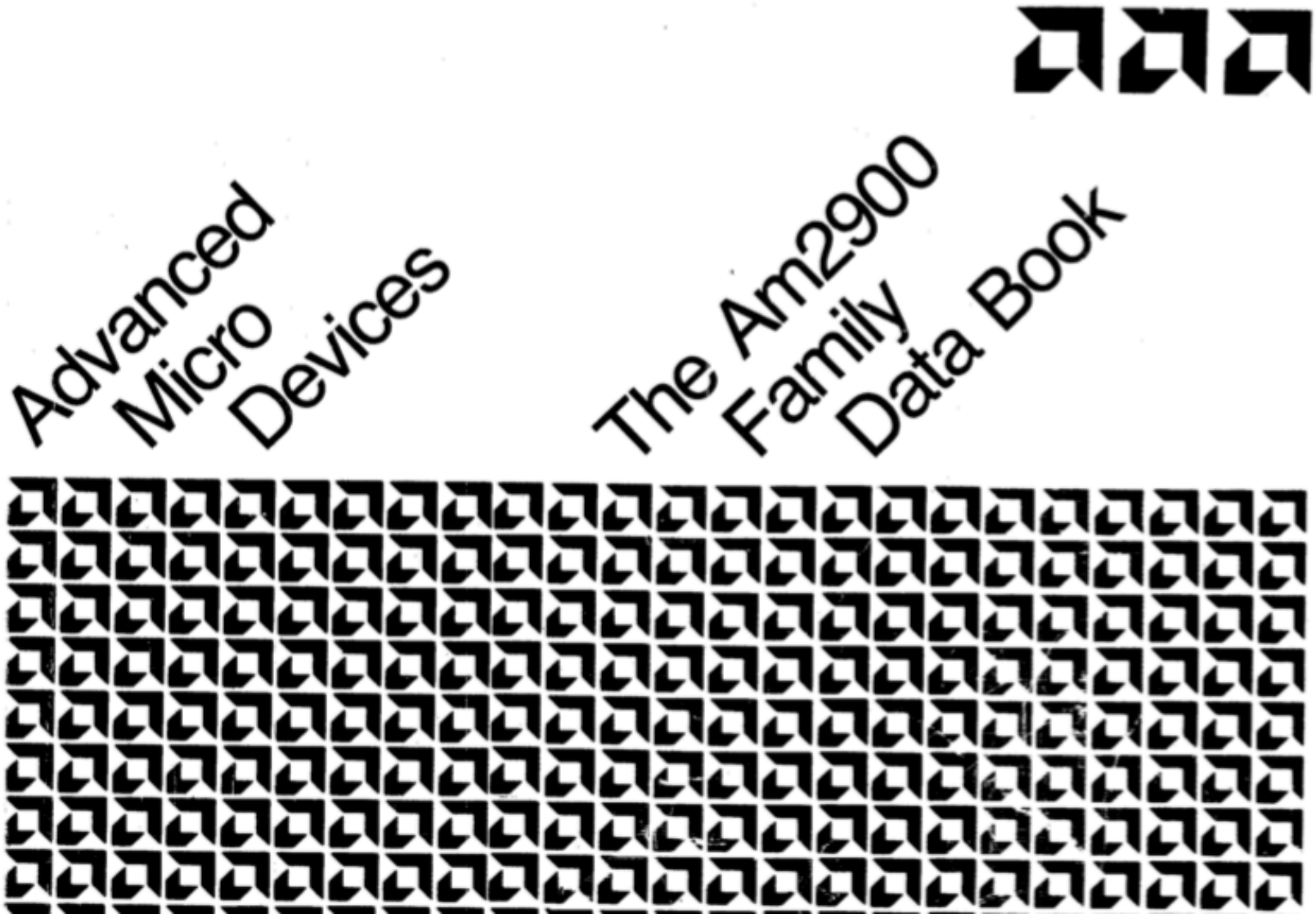
Am2900

Dr Jeff Drobman

website → drjeffsoftware.com/classroom.html

email → jeffrey.drobman@csun.edu

Am2900 Data Book



Am2900 Data Book

Advanced Micro Devices

The Am2900 Family Data Book With Related Support Circuits

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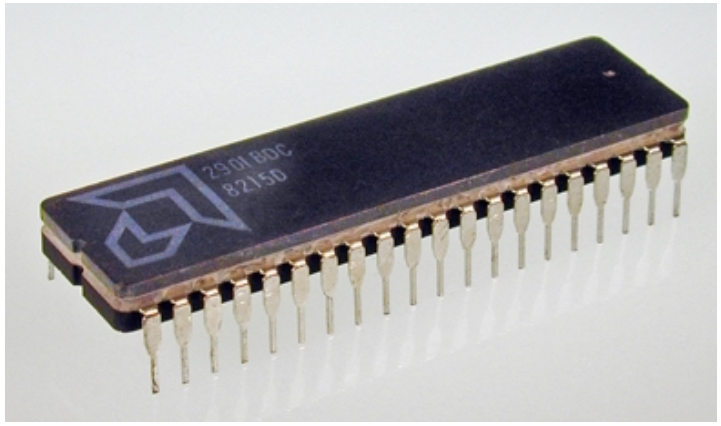
Am2900 Family

DR JEFF SOFTWARE
INDIE APP DEVELOPER

Bit-slice 1975-85

AMD 2901 bit-slice processor family includes 2901 and 2903 4-bit microprocessors slices, 2909 and 2911 microprogram sequencers, 2910 microprogram controller and other support chips. The 2901 processor consists of 16 4-bit registers, 4-bit ALU and associated decoding/multiplexing circuits. The ALU accepts 9-bit microinstructions that specify source operands, ALU function and the destination register. The 2901 ALU can perform 8 different functions (they are encoded into 3 bits within the microinstruction): addition, subtraction and logic operations. Multiple 2901 bit-slice processors could be combined together to build microprocessors with any data width (in 4 bits increments).

Enhanced version of 2901, AMD 2903 has 9 new special ALU functions used for implementation of multiplication, division and normalization operations. The number of arithmetic and logic ALU functions in 2903 was increased to 15.



AMD Am2903: 4-bit-slice ALU

Am2900 Family

Bit-slice 1975-85

Members of the Am2900 family [edit]

The Am2900 Family Data Book lists:[22]

- Am2901 – 4-bit bit-slice ALU (1975)
- Am2902 – Look-Ahead Carry Generator
- Am2903 – 4-bit-slice ALU, with hardware multiply
- Am2904 – Status and Shift Control Unit
- Am2905 – Bus Transceiver
- Am2906 – Bus Transceiver with Parity
- Am2907 – Bus Transceiver with Parity
- Am2908 – Bus Transceiver with Parity
- Am2909 – 4-bit-slice address sequencer
- Am2910 – 12-bit address sequencer
- Am2911 – 4-bit-slice address sequencer
- Am2912 – Bus Transceiver
- Am2913 – Priority Interrupt Expander
- Am2914 – Priority Interrupt Controller
- Am2915 – Quad 3-State Bus Transceiver
- Am2916 – Quad 3-State Bus Transceiver
- Am2917 – Quad 3-State Bus Transceiver
- Am2918 – Instruction Register, Quad D Register
- Am2919 – Instruction Register, Quad Register
- Am2920 – Octal D-Type Flip-Flop
- Am2921 – 1-to-8 Decoder
- Am2922 – 8-Input Multiplexer (MUX)
- Am2923 – 8-Input MUX
- Am2924 – 3-Line to 8-Line Decoder
- Am2925 – System Clock Generator and Driver
- Am2926 – Schottky 3-State Quad Bus Driver
- Am2927/Am2928 – Quad 3-State Bus Transceiver
- Am2929 – Schottky 3-State Quad Bus Driver
- Am2930 – Main Memory Program Control
- Am2932 – Main Memory Program Control
- Am2940 – Direct Memory Addressing (DMA) Generator
- Am2942 – Programmable Timer/Counter/DMA Generator
- Am2946/Am2947 – Octal 3-State Bidirectional Bus Transceiver
- Am2948/Am2949 – Octal 3-State Bidirectional Bus Transceiver
- Am2950/Am2951 – 8-bit Bidirectional I/O Ports
- Am2954/Am2955 – Octal Registers
- Am2956/Am2957 – Octal Latches
- Am2958/Am2959 – Octal Buffers/Line Drivers/Line Receivers
- Am2960 – Cascadable 16-bit Error Detection and Correction Unit
- Am2961/Am2962 – 4-bit Error Correction Multiple Bus Buffers
- Am2964 – Dynamic Memory Controller
- Am2965/Am2966 – Octal Dynamic Memory Driver

2900 Family

Am2900

II. 2900 Family Products

Am2901/A/B	4-Bit Bipolar Microprocessor Slice
	Using the Am2901
Am2901C	Improved-Speed 4-Bit Microprocessor Slice
Am2902A	High-Speed Look-Ahead Carry Generator
Am2903/29203	The Superslice® (Advanced 4-Bit Bipolar Microprocessor Slice)
	Using the Am2903 and Am29203
	Am2903 Detailed Switching Characteristics
Am2903A	Improved Speed Superslice™
Am2904	Status and Shift Control Unit
Am2905	Quad 2-Input OC Bus Transceiver with 3-State Receiver
Am2906	Quad 2-Input OC Bus Transceiver with Parity
Am2907/2908	Quad Bus Transceiver with Interface Logic
Am2909/2909A	Microprogram Sequencer
Am2910	Microprogram Controller
Am2911/2911A	Microprogram Sequencer
Am2912	Quad Bus Tranceiver
Am2913	Priority Interrupt Expander
Am2914	Vectored Priority Interrupt Controller
	A Microprogrammable Interrupt Structure
	Priority Interrupt Encoder Logic Description
Am2915A	Quad 3-State Bus Transceiver with Interface Logic
Am2916A	Quad 3-State Bus Transceiver with Interface Logic
Am2917A	Quad 3-State Bus Transceiver with Interface Logic
Am2918	Quad D Register with Standard and 3-State Outputs
Am29LS18	Quad D Register with Standard and 3-State Outputs
Am2919	Quad Register with Dual 3-State Outputs
Am2920	Octal D-Type Flip-Flop with Clear, Clock Enable and 3-State Control

2900 Family

Am2900

Am29112	Interruptable 8-Bit Microprogram Sequencer
	Am2900 High Performance Controller Products
Am29116	16-Bit Bipolar Microprocessor
	Am2900 High Performance Controller Products
Am29700/701	Non-Inverting Schottky 64-Bit Random Access Memories
Am29702/703	Schottky 64-Bit Random Access Memories
Am29705	16-Word by 4-Bit 2-Port RAM
Am29705A	Improved Speed 2-Port RAM
Am29720/721	Low-Power Schottky 256-Bit Random Access Memories
Am29750/751A	32-Word by 8-Bit PROMs
Am29760A/761A	256-Word by 4-Bit PROMs
Am29770/771	2048-Bit Generic Series Bipolar PROM
Am29774/775	4096-Bit Generic Series Bipolar PROM with Output Register
Am29803A	16-Way Branch Control Unit
Am29811A	Next Address Control Unit

Am2901 • Am2901A • Am2901B

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.
- Fast –
  Am2901B is up to 27% faster than Am2901A, up to 50% faster than Am2901. The Am2901B meets or exceeds all of the specifications for the Am2901 and Am2901A.

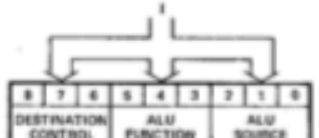
GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

The Am2901B is a plug-in replacement for the Am2901 or Am2901A, but is 25% faster than the Am2901A and 50% faster than the Am2901.

MICROPROCESSOR SLICE BLOCK DIAGRAM



Logic History

Am2900

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10-20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

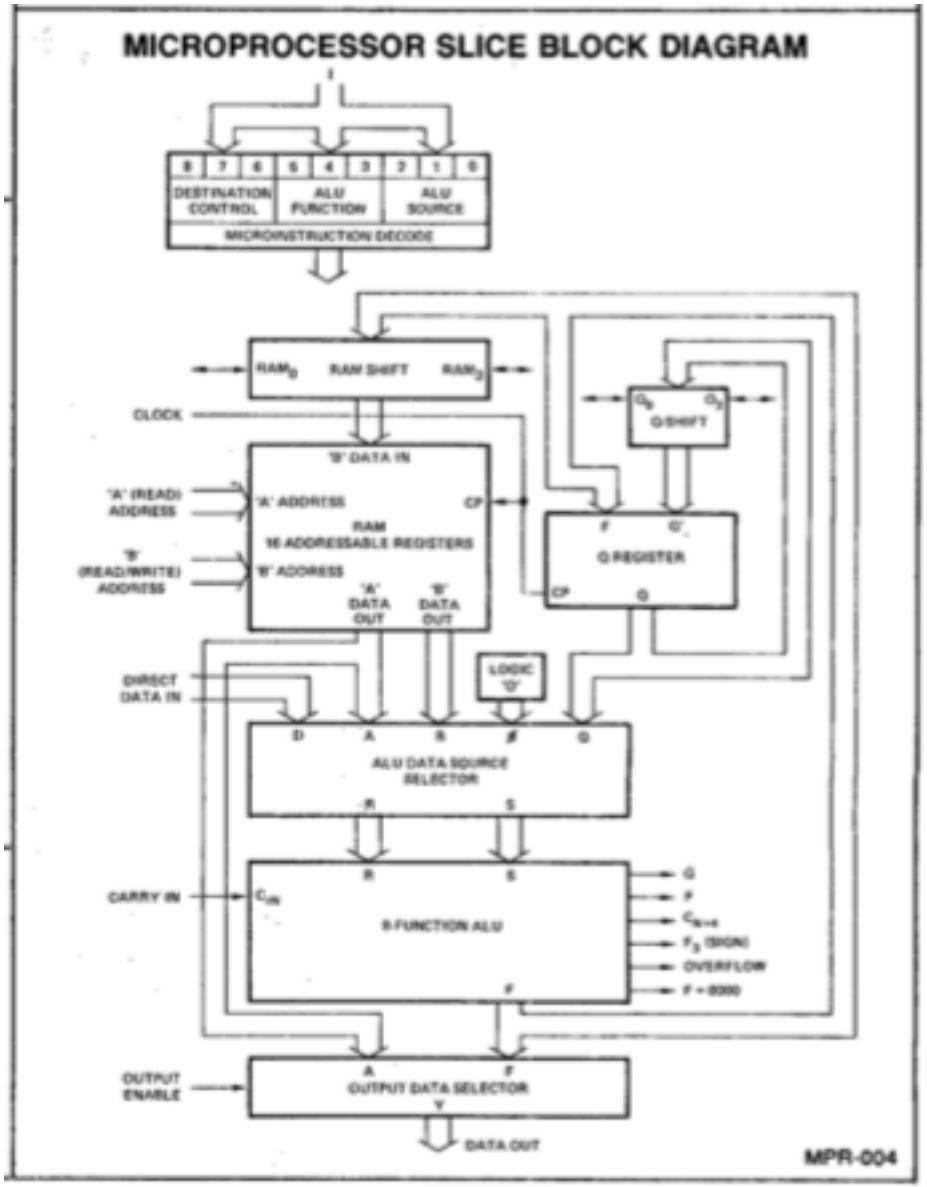
- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20-50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic is around 500 gates/chip.

GENERATION III – The Am2900 Family, 1976

2901 Block Diagram

Am2900



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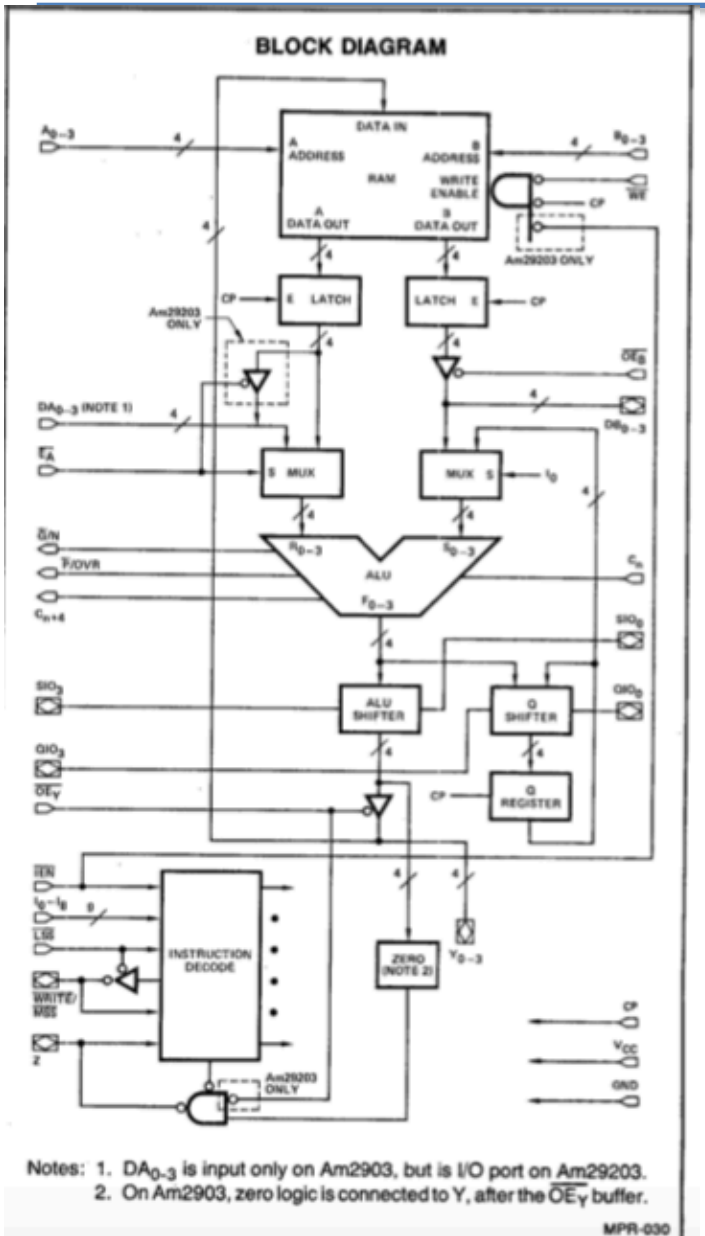
2901 Block Diagram

Am2900



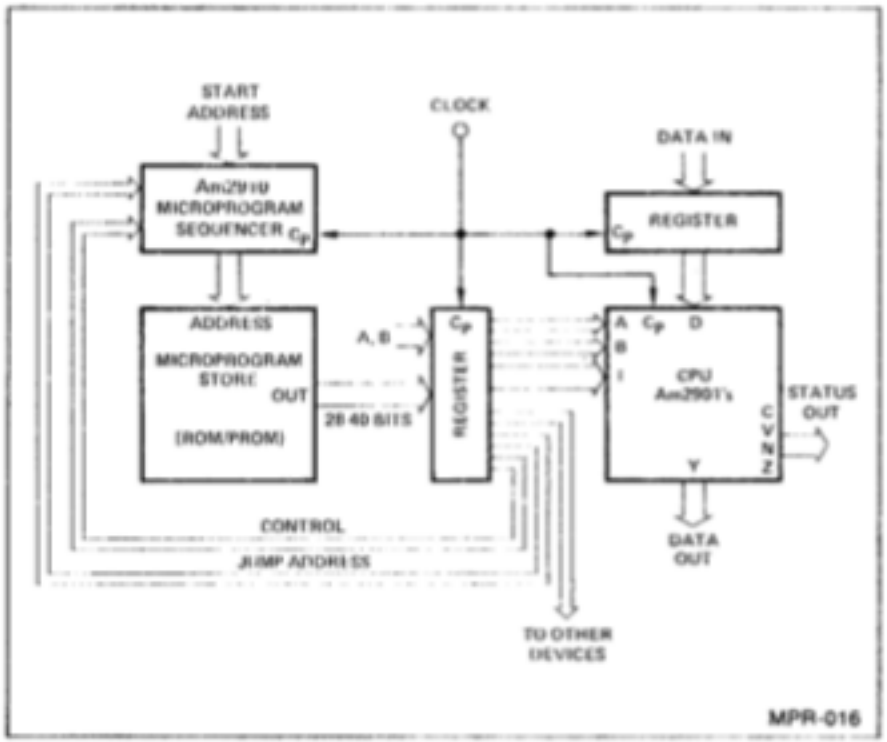
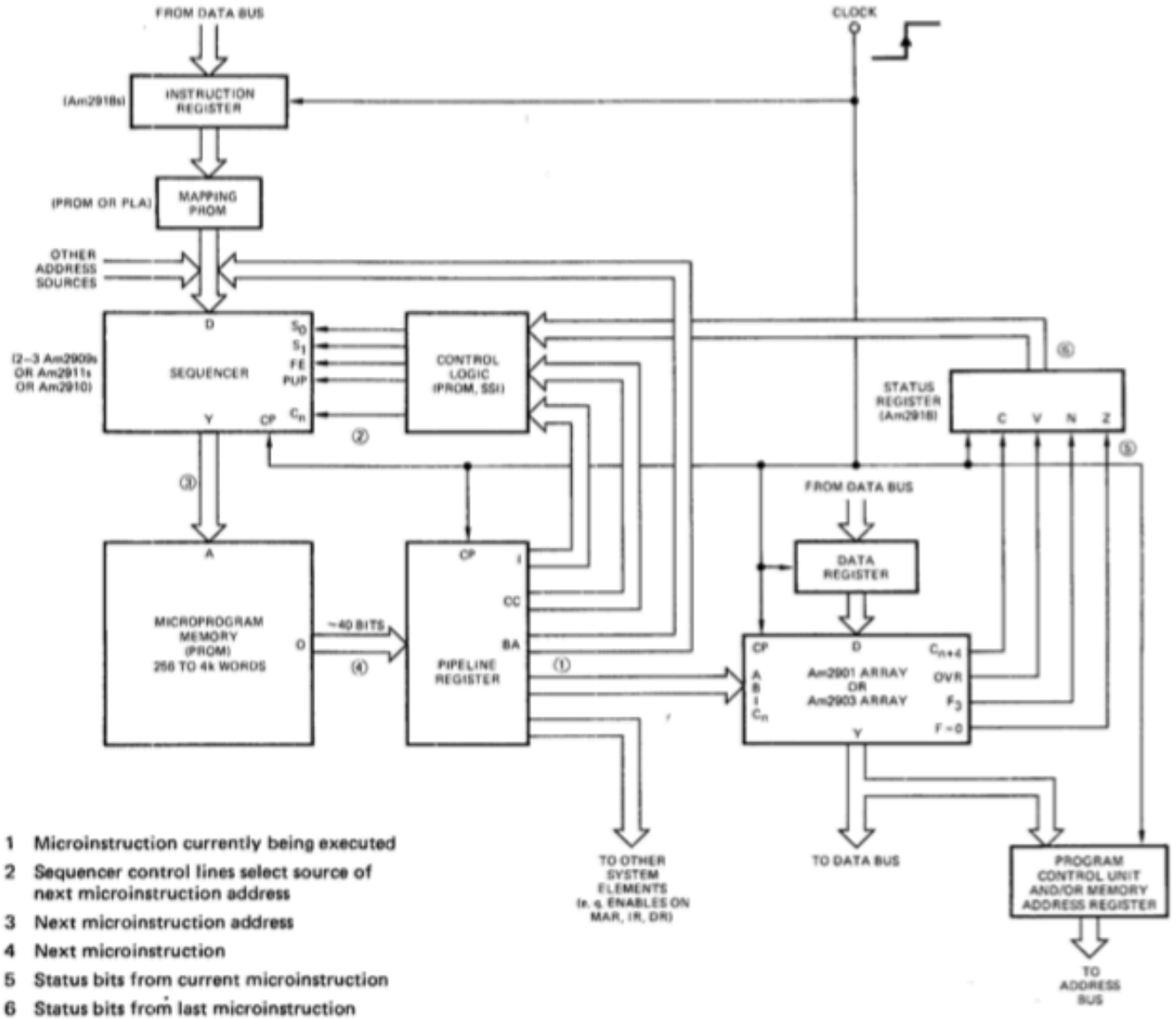


Figure 15. Microprogrammed Architecture Around Am2901's.

System Block Diagram

2900 System Block Diagram

Am2900



2901 Block Diagram

Am2900

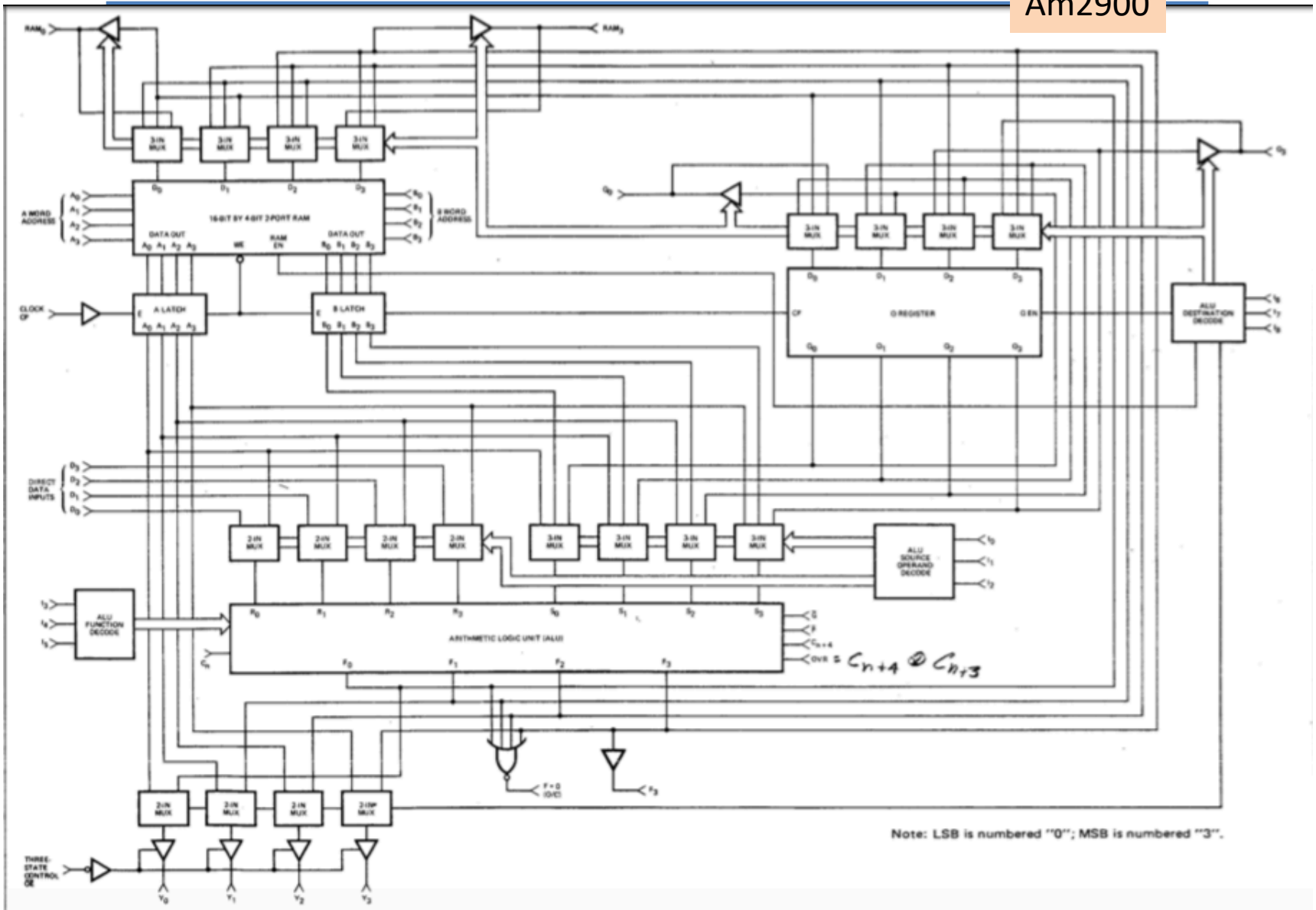


Figure 1. Detailed Am2901B Microprocessor Block Diagram.

MPR-005

2901 8 ALU Ops

Am2900

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX OR S	R ∀ S
EXNOR	H	H	H	7	R EX NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
□ RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
✳ RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
△ RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

✳ DON'T USE □ DISABLE $\overline{FEN}$ △ ENABLE $\overline{FEN}$

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

2901 8 ALU Ops

Am2900

OCTAL I_{210}	OCTAL I_{543} ALU Function \ ALU Source	0 A, Q	1 A, B	2 O, Q	3 O, B	4 O, A	5 D, A	6 D, Q	7 D, O
0	C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	$\overline{A}$∧B	Q	B	A	$\overline{D}$∧A	$\overline{D}$∧Q	0
6	R EX-OR S	A∀Q	A∀B	Q	B	A	D∀A	D∀Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

2901 8 ALU Ops

Am2900

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0\,(G_0 + \overline{C_n})}$	Seenote

Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

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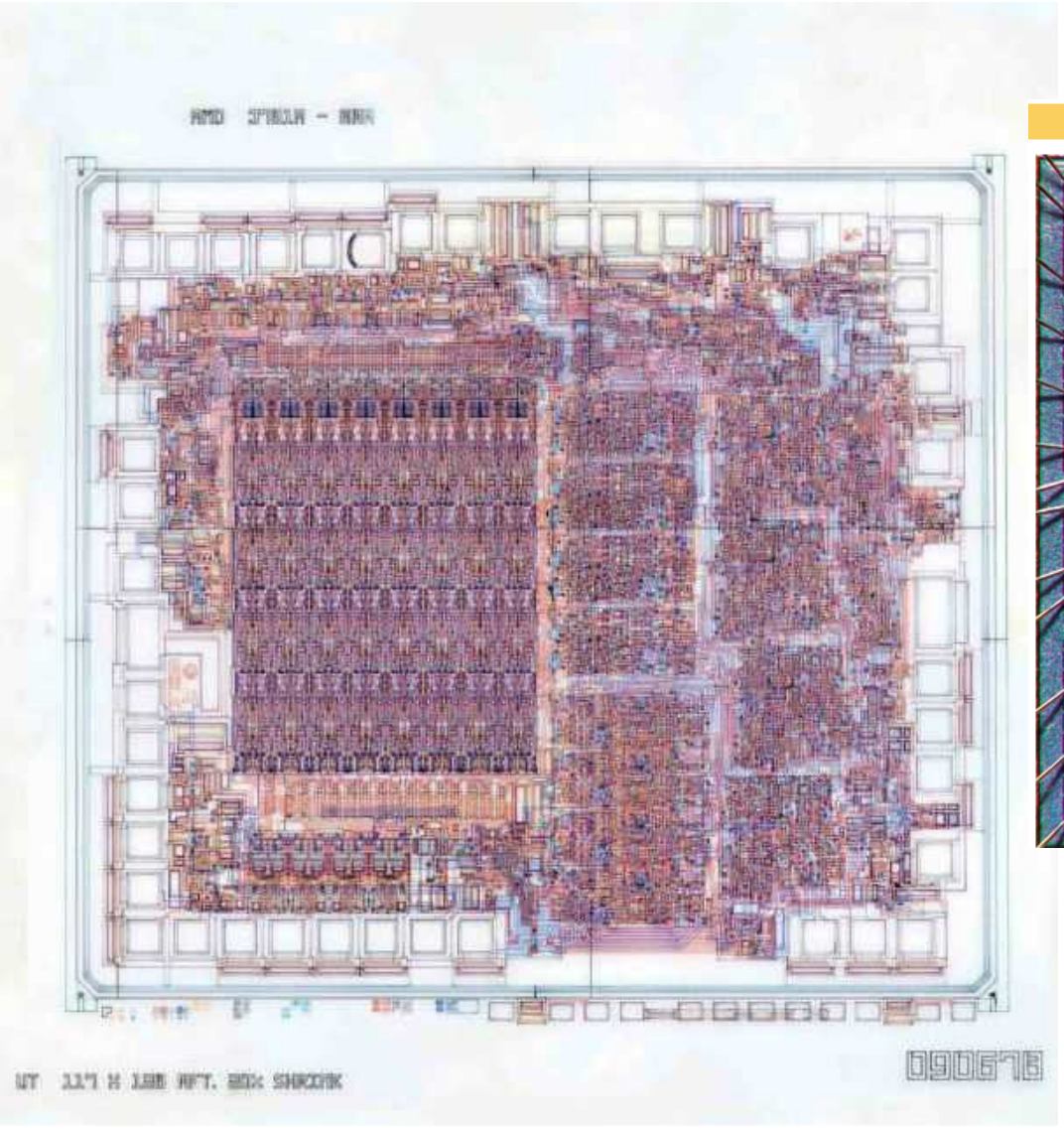
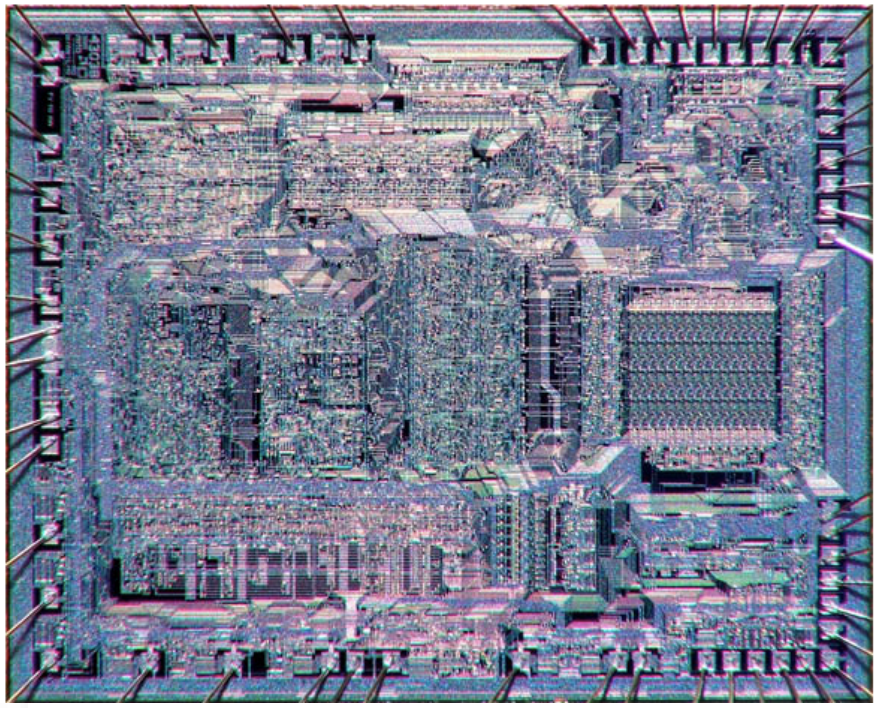
Am2901/3 4-bit MPU

Bit-slice 1975-85

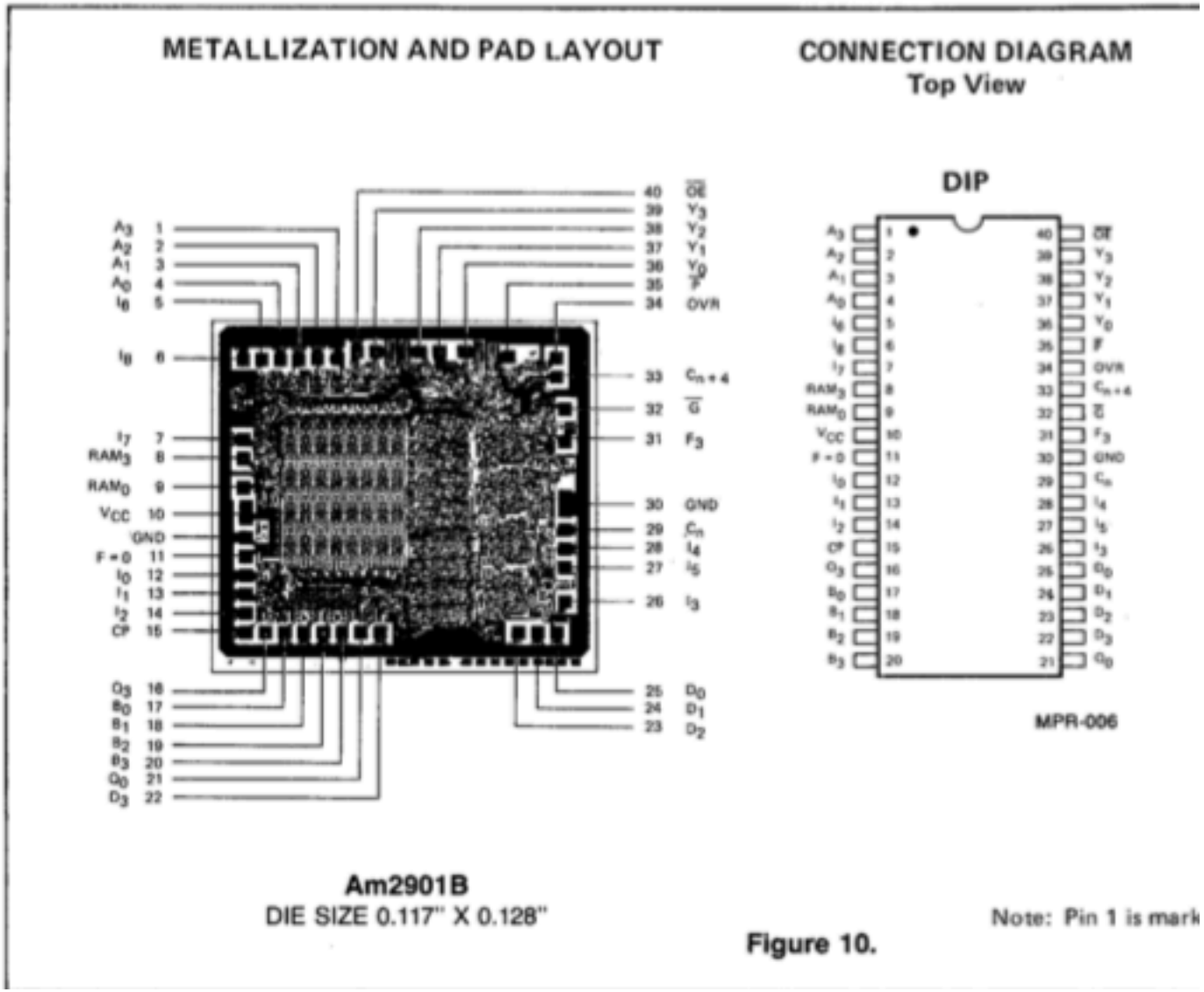


AMD AM2903ADC



2901 Chip

Am2900

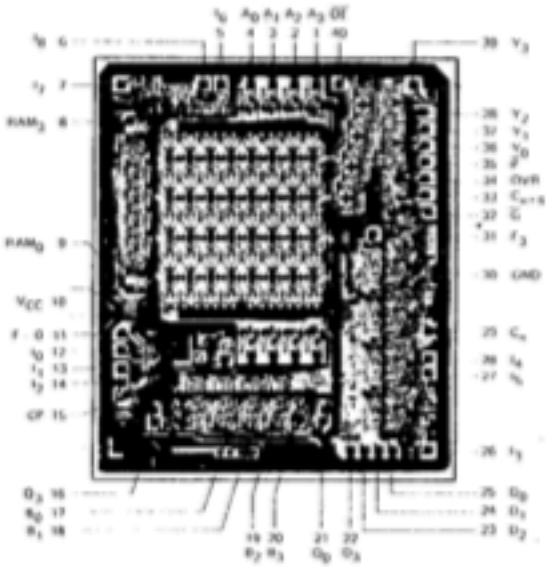


2901-A-B Die

Am2900

SMALLER DIE SIZES MAKE FASTER PARTS

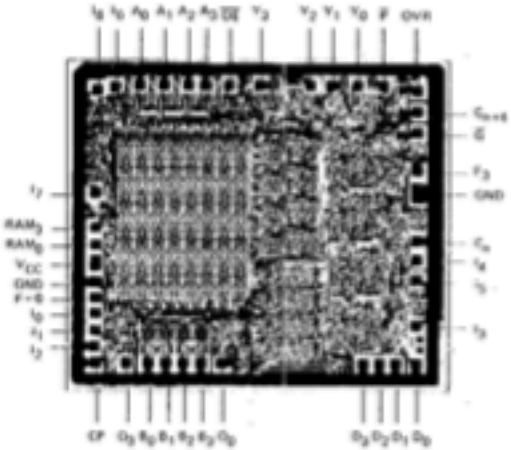
Am2901



DIE SIZE 0.167" X 0.198"

Speed A,B → $\overline{G}$,$\overline{P}$ 80ns

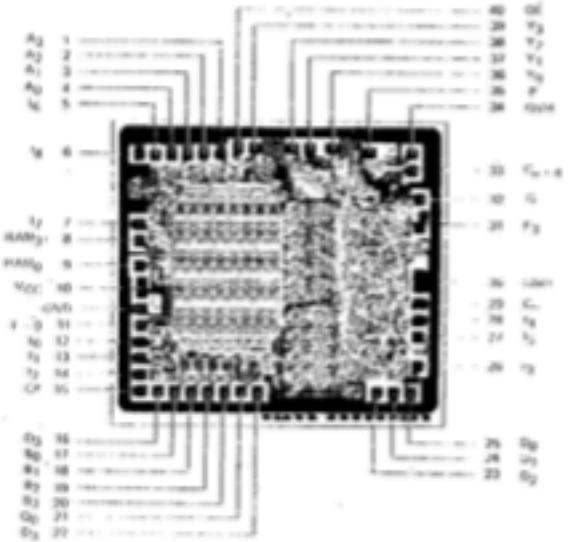
Am2901A



DIE SIZE 0.132" X 0.149"

Speed A,B → $\overline{G}$,$\overline{P}$ 65ns

Am2901B

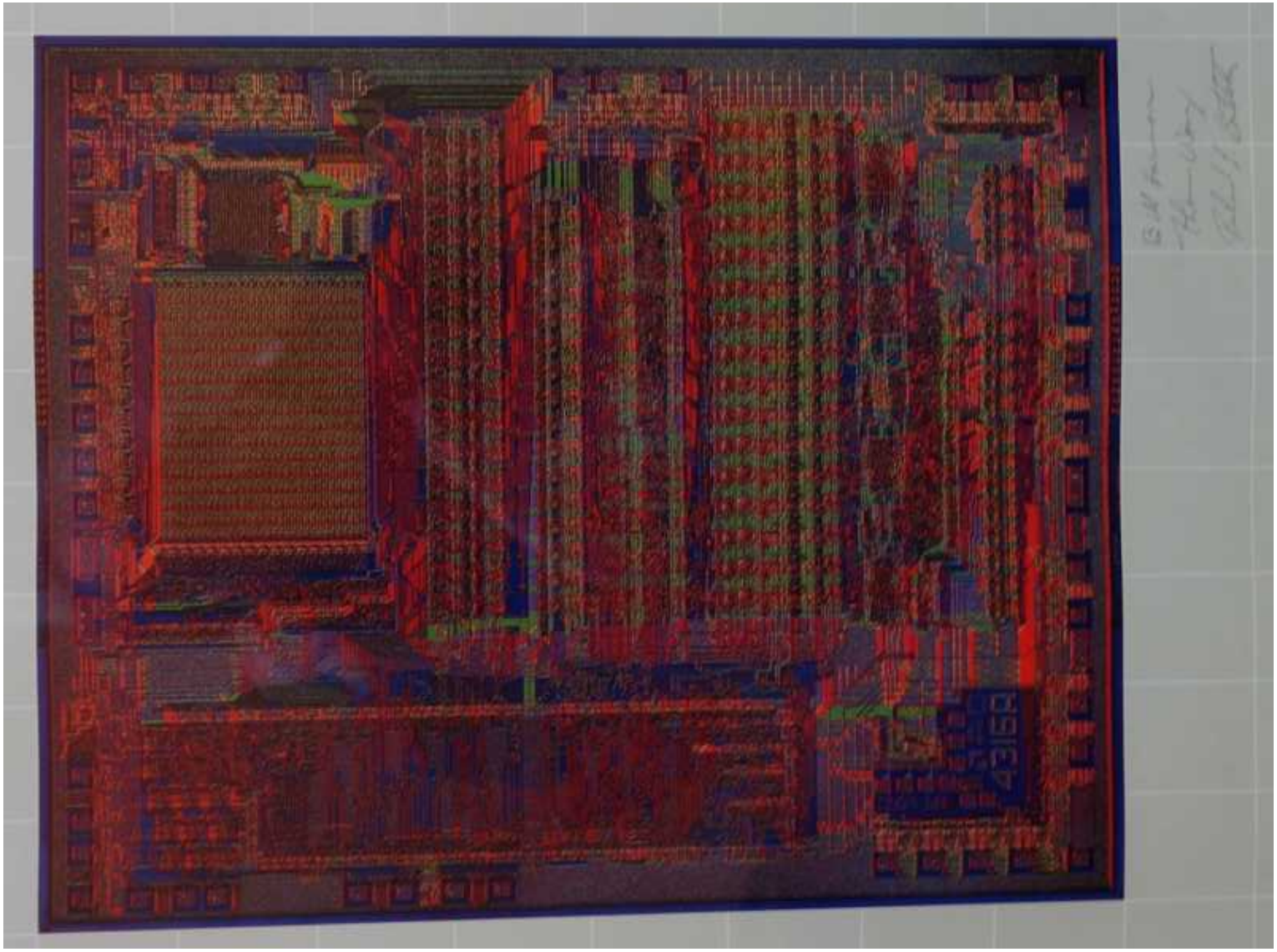


DIE SIZE 0.117" X 0.128"

Speed A,B → $\overline{G}$,$\overline{P}$ 50ns

Am29116 16-bit MPU

Bit-slice | 1985-88



Vcc & Temp

Am2900

OPERATING RANGE

Part Number Suffix	V_{CC}	Temperature
PC, PCB, DC, DCB XC	4.75V to 5.25V	T_A = 0°C to +70°C
DM, DMB FM, FMB XM	4.50V to 5.50V	T_C = −55°C to +125°C

- Com'l
- Mil

2901 Variants

Am2900

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2901 Order Number	Am2901A Order Number	Am2901B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2901PC	AM2901APC	AM2901BPC	P-40	C	C-1
AM2901DC	AM2901ADC	AM2901BDC	D-40	C	C-1
AM2901DC-B	AM2901ADC-B	AM2901BDC-B	D-40	C	B-2 (Note 4)
	AM2901ADM	AM2901BDM	D-40	M	C-3
	AM2901ADM-B	AM2901BDM-B	D-40	M	B-3
	AM2901AFM	AM2901BFM	F-42	M	C-3
	AM2901AFM-B	AM2901BFM-B	F-42	M	B-3
	AM2901AXC	AM2901BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
	AM2901AXM	AM2901BXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Figure 9.

12-bit CPU = 3x 2901

Am2900

Ripple Carry

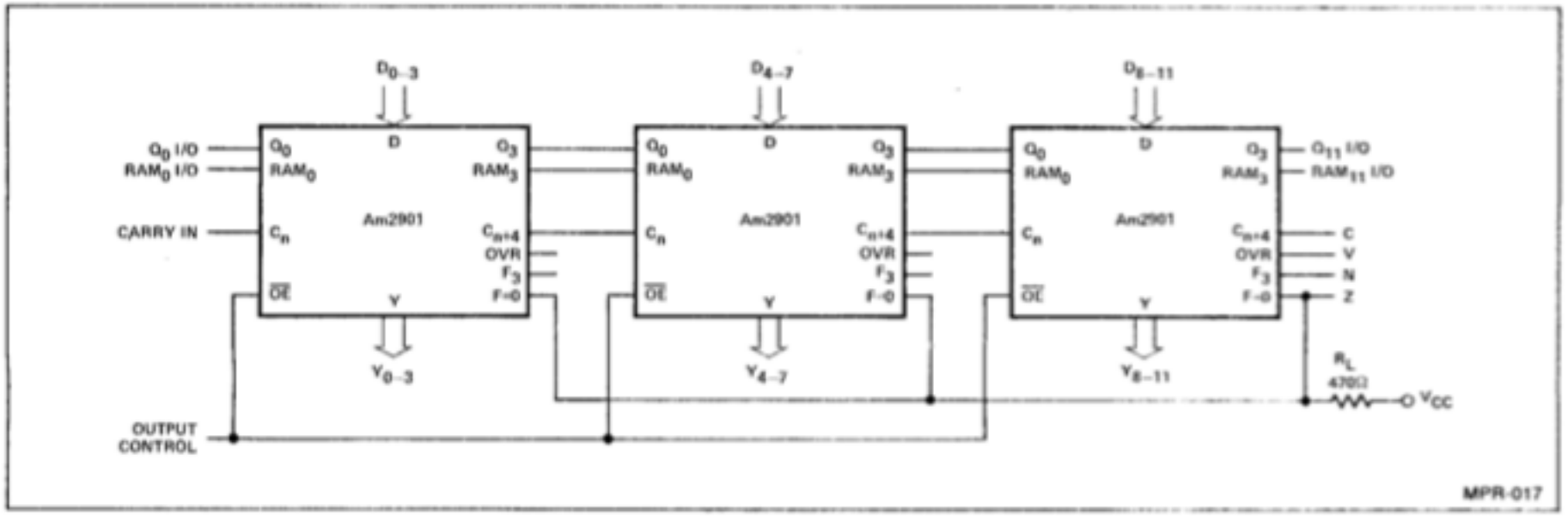


Figure 16. Three Am2901's used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected Together.

Am2902 CLA

Am2900

Am2902A

High-Speed Look-Ahead Carry Generator

DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries across a group of four Am2901 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 4.5 ns
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902A is generally used with the Am2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

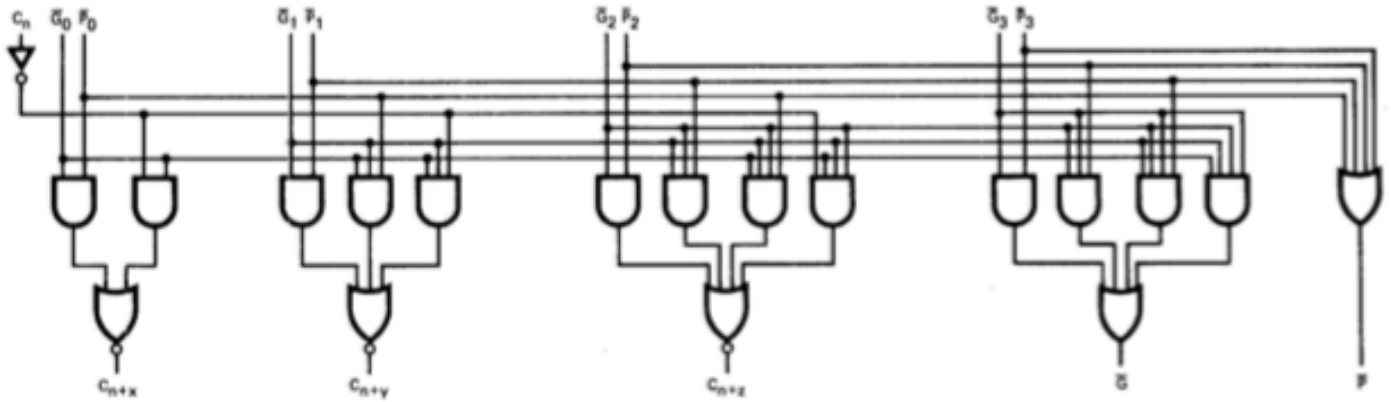
The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

Am2902 CLA

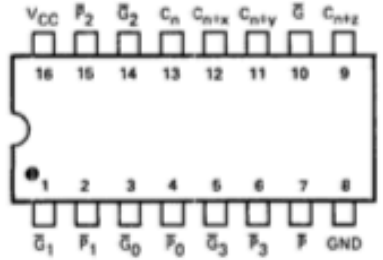
Am2900

LOGIC DIAGRAM



MPR-026

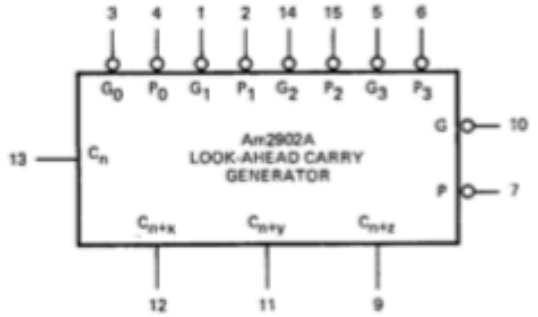
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-027

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-025

16-bit CPU = 4x 2901

Am2900

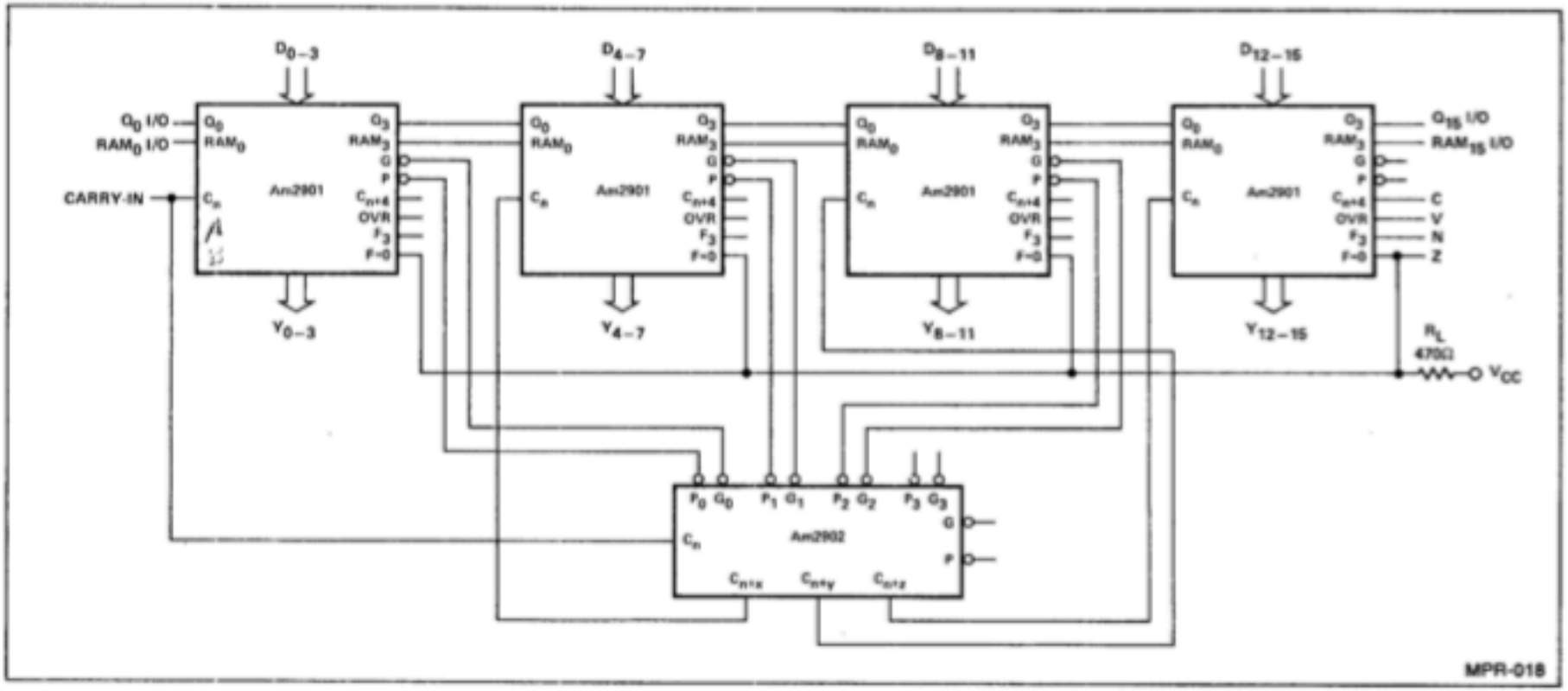


Figure 17. Four Am2901s in a 16-Bit CPU Using the Am2902 for Carry Lookahead.

48-bit CPU = 12x 2901

Am2900

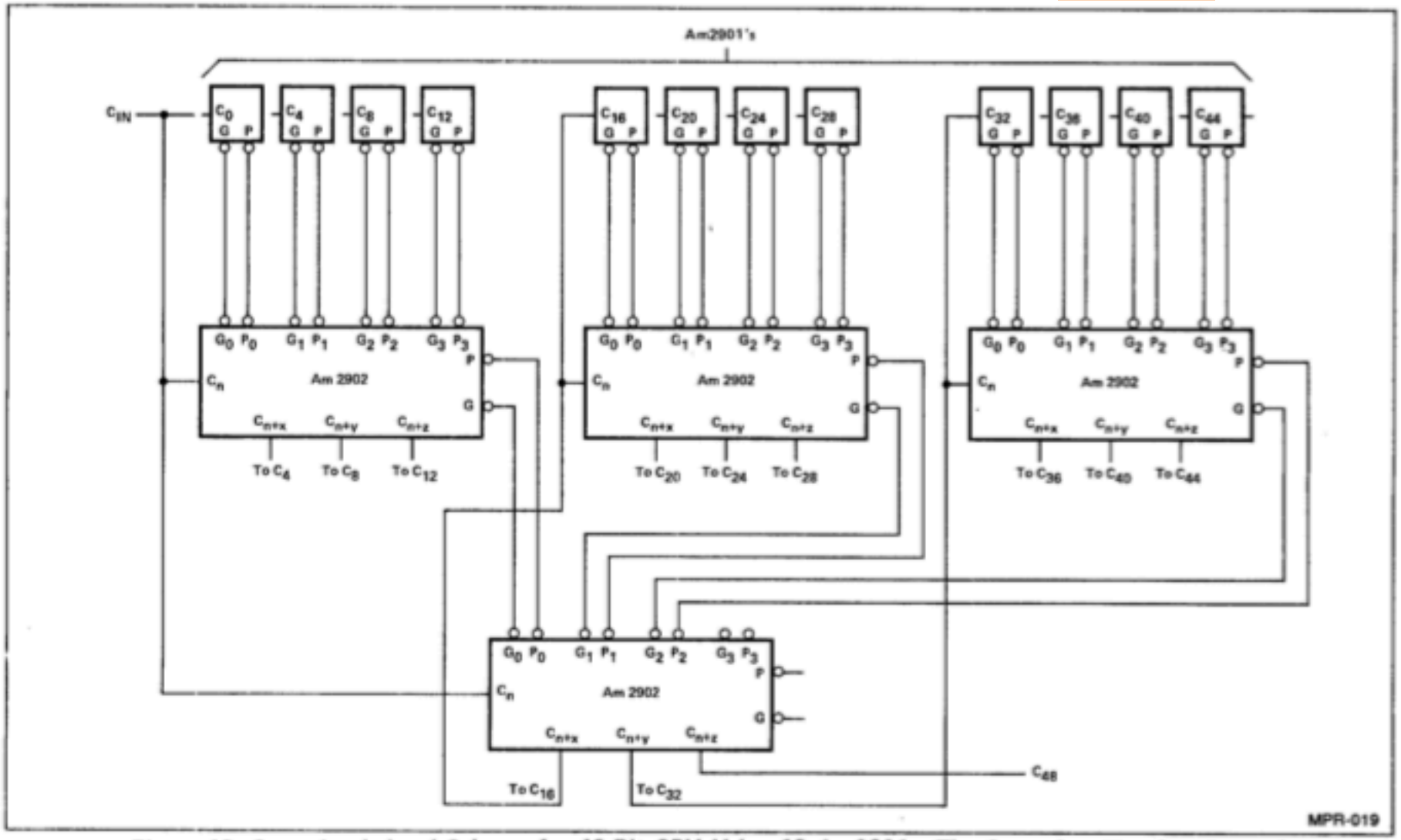


Figure 18. Carry Lookahead Scheme for 48-Bit CPU Using 12 Am2901s. The Carry-Out Flag (C_{48}) Should be Taken From the Lower Am2902 Rather Than the Right-Most Am2901 for Higher Speed.

DC Specs

Am2900

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
			I_{OH} = −1.0mA, C_{n+4}	2.4			
			I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
			I_{OH} = −600μA, F_3	2.4			
			I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
			I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}				250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3 I_{OL} = 20mA (COM'L)			0.5	Volts
			I_{OL} = 16mA (MIL)			0.5	
		$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
		C_{n+4}	I_{OL} = 10mA			0.5	
		OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
		F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	Clock, $\overline{OE}$			−0.36	mA
			A_0, A_1, A_2, A_3			−0.36	
			B_0, B_1, B_2, B_3			−0.36	
			D_0, D_1, D_2, D_3			−0.72	
			I_0, I_1, I_2, I_6, I_8			−0.36	
			I_3, I_4, I_5, I_7			−0.72	
			$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
			C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	Clock, $\overline{OE}$			20	μA
			A_0, A_1, A_2, A_3			20	
			B_0, B_1, B_2, B_3			20	
			D_0, D_1, D_2, D_3			40	
			I_0, I_1, I_2, I_6, I_8			20	
			I_3, I_4, I_5, I_7			40	
			$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
			C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA

Multiply & Shift

Am2900

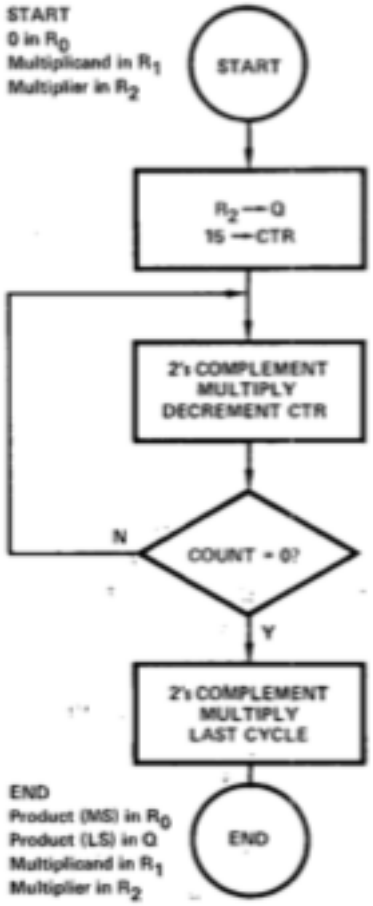
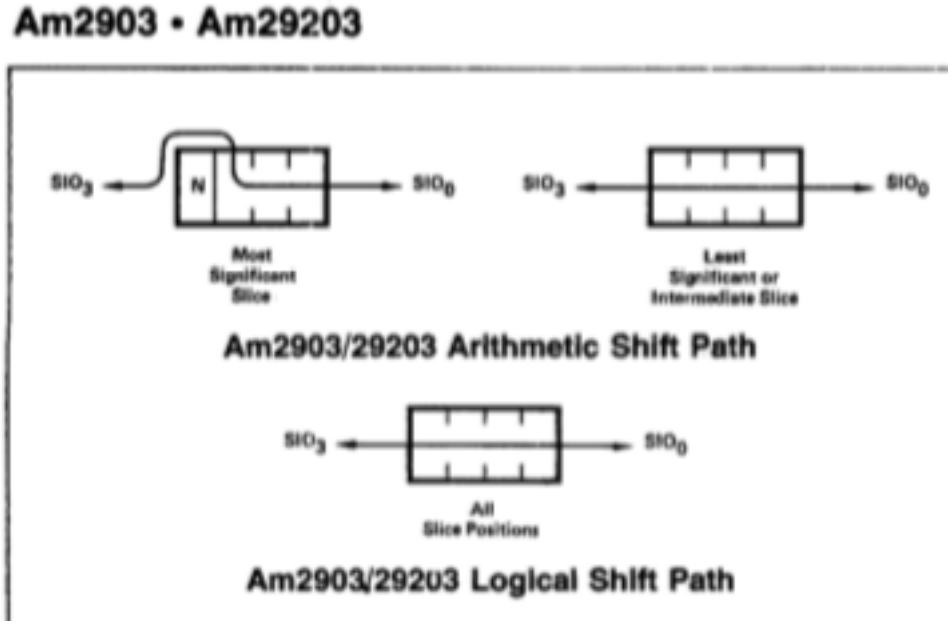


Figure 14. 2's Complement 16 X 16 Multiply.



Division

Am2900

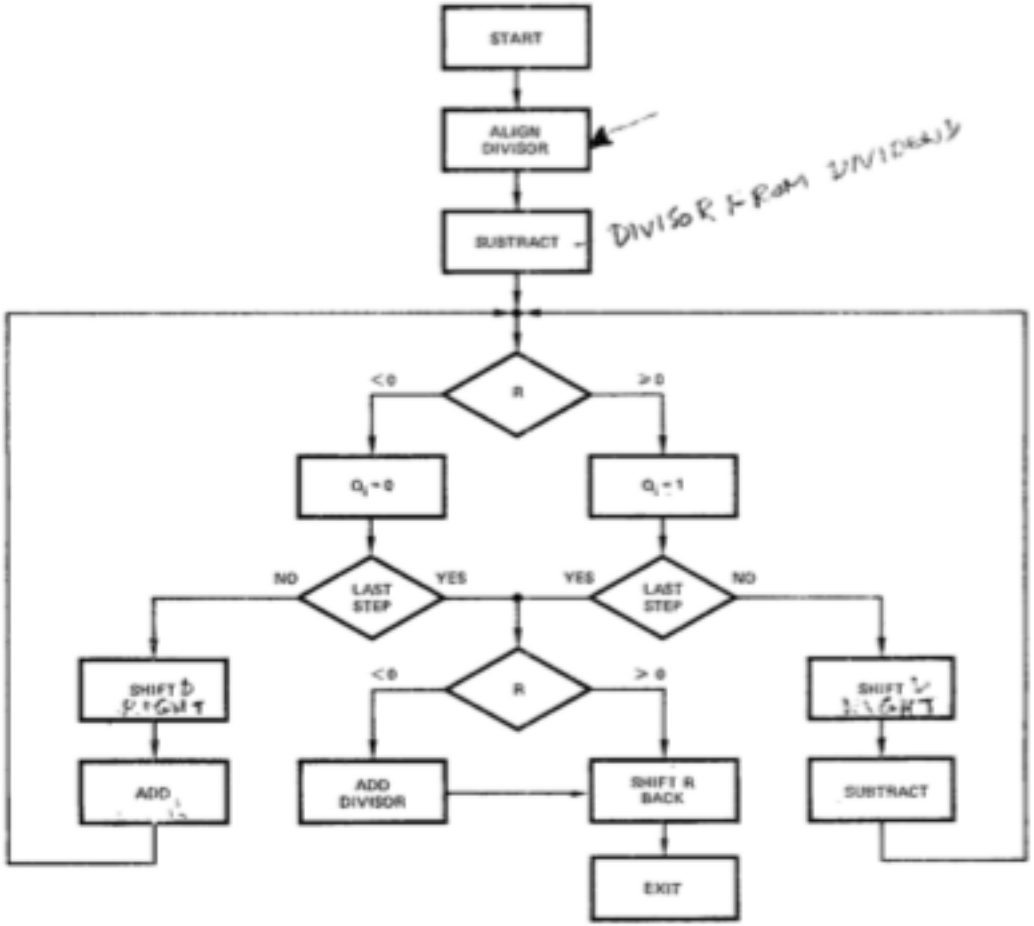


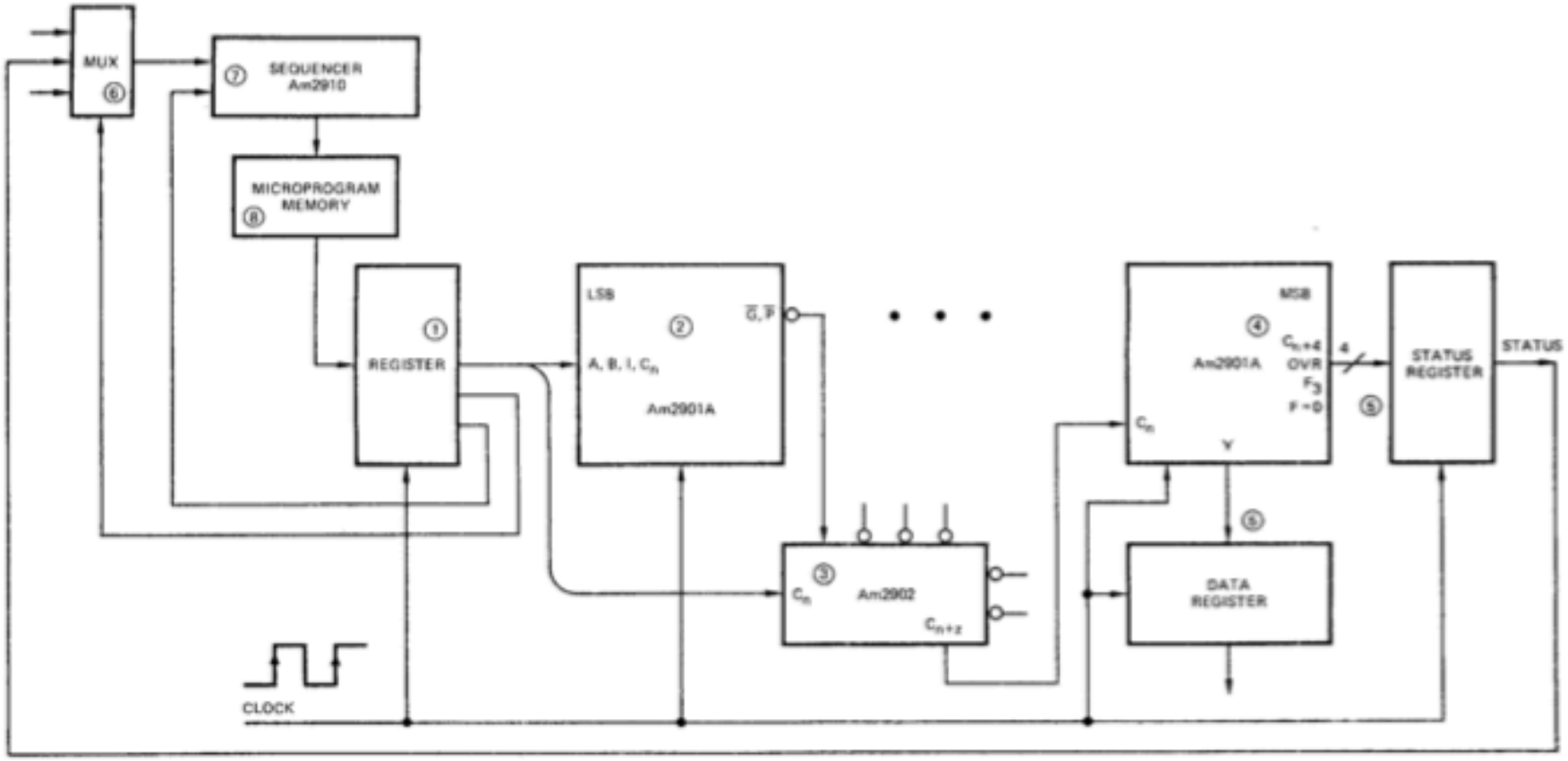
Figure 22. Flowchart for Non-Restoring Division (Unsigned Numbers).

Timing – Cycle Times

Am2900

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



Timing

Am2900

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↓	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	–	–	16	0

Timing – Logic

Am2900

TABLE IV E-2
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Multiply Instruction
(I_{8765} = 2_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	113	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	78	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	85	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	58	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	105	97	–	–	89	102	–	–	•	71 •	•	–
	IS	105	97	81	–	–	–	–	–	•	71 •	•	–
	LSS	105	97	81	42	–	–	–	53	•	71 •	•	–
I_{4321}	MSS	112	98	–	–	94	111	–	–	•	75 •	•	–
	IS	112	98	85	–	–	–	–	–	•	75 •	•	–
	LSS	112	98	85	43	–	–	–	53	•	75 •	•	–
I_{8765}	MSS	99	86	–	–	78	100	–	–	•	74 •	•	–
	IS	99	86	84	–	–	–	–	–	•	74 •	•	–
	LSS	99	86	84	48	–	–	–	50	•	74 •	•	–
Clock	MSS	107	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	57	–	–	39	–	42	91	–	–
Z	MSS	90	65	–	–	70	81	–	–	–	72	–	–
	IS	90	65	48	–	–	–	–	–	–	72	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

F = S + C_n if Z = 0
S + R + C_n is Z = 1
Y_3 = F_3 ⊕ OVR (MSS)
Z = Q_0 (LSS)

Timing – Clocked

Am2900

TABLE IV B
Guaranteed Set-up and Hold Times
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	23	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	35	0	To Write into RAM
A, B as Sources	Clock	38	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	23	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	74	0	See Note 6

Notes:

1. For set-up times from all inputs not specified in Table IV B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

Am2903 Upgrade

Am2900

Am2903 • Am29203

The Superslice®

DISTINCTIVE CHARACTERISTICS

- Expandable Register File –
  Like the Am2901, the Am2903/29203 contains 16 internal working registers arranged in a two-address architecture. But the Am2903/29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- Built-in Multiplication Logic –
  Performing multiplication with the Am2901A requires a few external gates – these gates are contained on-chip in the Am2903/29203. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- Built-in Division Logic –
  The Am2903/29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- Built-in Normalization Logic –
  The Am2903/29203 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- Built-in Parity Generation Circuitry –
  The Am2903/29203 can supply parity across the entire ALU output for use in error detection.
- Built-in Sign Extension Circuitry –
  To facilitate operation on different length two's complement numbers, the Am2903/29203 provides the capability to extend the sign at any slice boundary.
- BCD Arithmetic (Am29203 only) –
  Automatic BCD add and subtract and conversion between binary and BCD.
- Improved Byte Handling (Am29203 only) –
  Zero detection and register writing can be performed on a single byte rather than the whole word.

GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am29203 is a similar device, but has additional I/O capability, more special instructions and will be at least 30% faster.

BLOCK DIAGRAM