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# Technology

DR JEFF SOFTWARE
INDIE APP DEVELOPER



Fall 2023 Rev 7-21-23

## IC Technology

# Transistors

Dr Jeff Drobman

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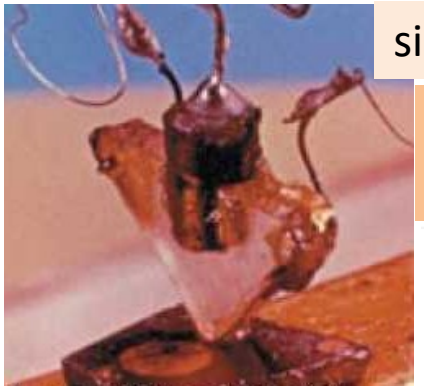
email → jeffrey.drobman@csun.edu

# The Transistor



size = ~1 inch

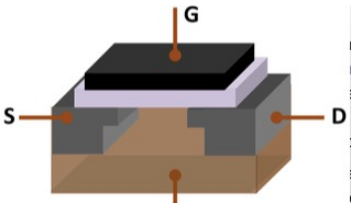
**1947** ushered in the era of ***Microelectronics***

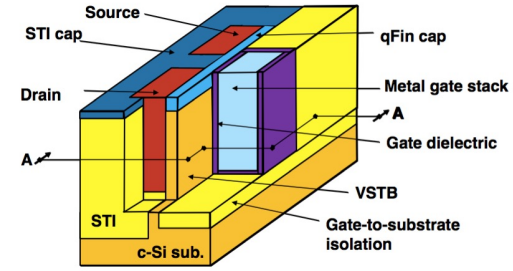
A **transistor** is a semiconductor device used to amplify or switch electronic signals and electrical power. It is composed of semiconductor material usually with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor's termina


- 1947- Bipolar point/junction
- 1959- Planar bipolar [10]*
- 1964- MOS (P-channel) [100]
- 1972- MOS (N-channel) [1,000]
- 1978- CMOS [4,000]
- 1990- sub-micron [10,000]
- 2000- 100 nm [100,000]
- 2011- FinFET [1,000,000]
- 2019- 7nm [10,000,000,000]

*no. of transistors

Transistors have been shrunk every 2 years according to ***Moore's Law***




- size = 10 nm = $4 \times 10^{-7}$ inches
- yields → ~1M devices per $cm^2$

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# Viewing Transistors

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Quora

## How are billions of transistors compressed into a single chip? Can a transistor in the chip be seen with a microscope?

**Jeff Drobman**
Works at Dr Jeff Software · Just now ·

once a chip is complete, only the top few layers of metal interconnect are visible (unless etched away). a single transistor is way too small to be readily identified, as they are now as small as about 25–40 nm in overall size. note that a “5nm” node means that only the channel length is that small. the overall transistor size, and pitch, is more like 25–40 nm.

# Transistor Atoms




Quora

**Al Kordesch**, Semiconductor Device Modeling

Answered Feb 1, 2019

**How many atoms are in a typical transistor in a chip?**

**Short Answer: 49,000 atoms!**

**Apple's iPhone XS uses 7 nanometer transistors.** So let's estimate how many atoms are in one of them. Excluding the connecting wires and other parts, I'm just going to calculate the size of the active part, the "channel" under the gate. The volume of the channel is about (7 nm long) x (7 nm deep) x (20 nm wide). The atomic density of silicon is 5E+28 atoms per cubic meter. So let's go!

Number of atoms n = volume x density

n = (980E-27) x (5E+28) = 49,000 atoms.

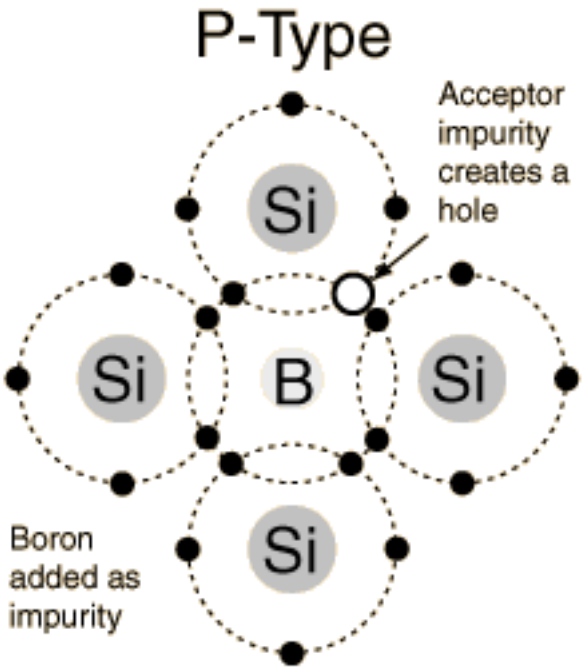
Atomic radius = .111nm → 4.5 atoms/nm → 5/nm

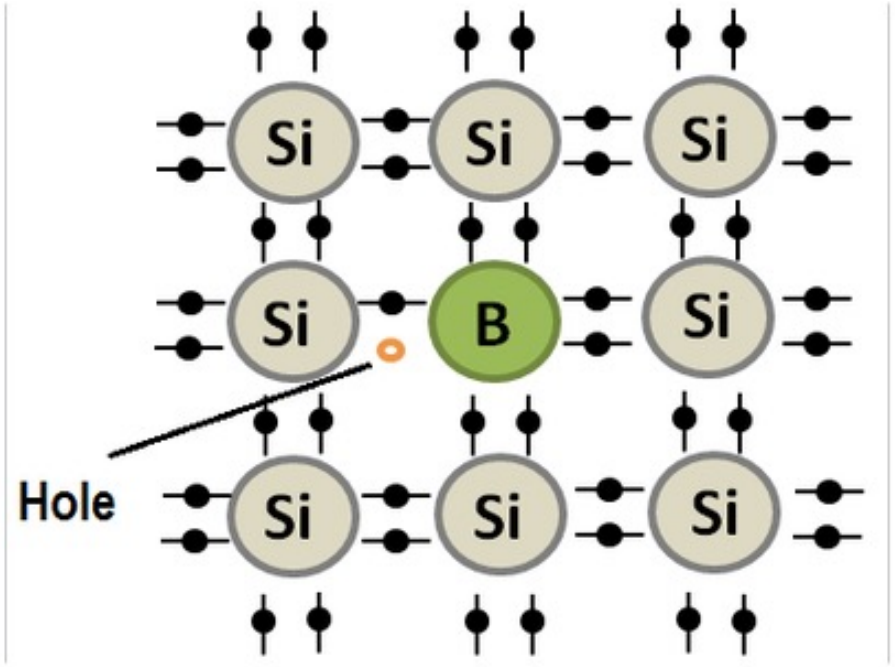
Cubic: 5x5x5 = **125** atoms/cu nm

@7n: ~1000 cu nm

# P-type Semi






(Source: Doped Semiconductors)

- Majority carrier = ***Holes*** slow
- Electron ***Acceptor***

# IC Process & Interface



**TTL** compatible — **5V → 3V**

## ❖ *Bipolar*

**5V**

- RTL→DTL→TTL → *Schottky* TTL→ *LS* TTL

| 1960 | 1965 | 1970 | 1975 | 1980 | 1985 | 1990 |
|---|---|---|---|---|---|---|

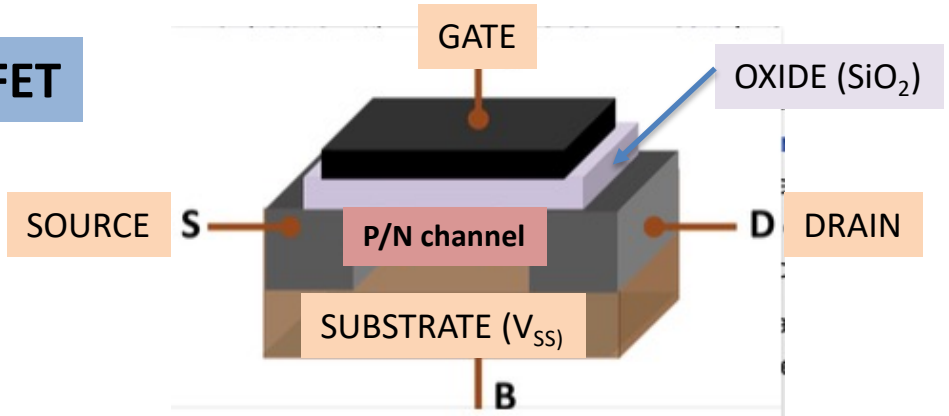
## ❖ *MOS*

- PMOS→NMOS → **CMOS** → CMOS (TTL I/O)→ 3.3V

***BiCMOS***

**5V → 3V**

**MOSFET**




The **metal–oxide–semiconductor field-effect transistor**, also known as the **metal–oxide–silicon transistor**, is a type of field-effect transistor that is fabricated by the controlled oxidation of a semiconductor, typically silicon. It has an insulated gate, whose voltage determines the conducti

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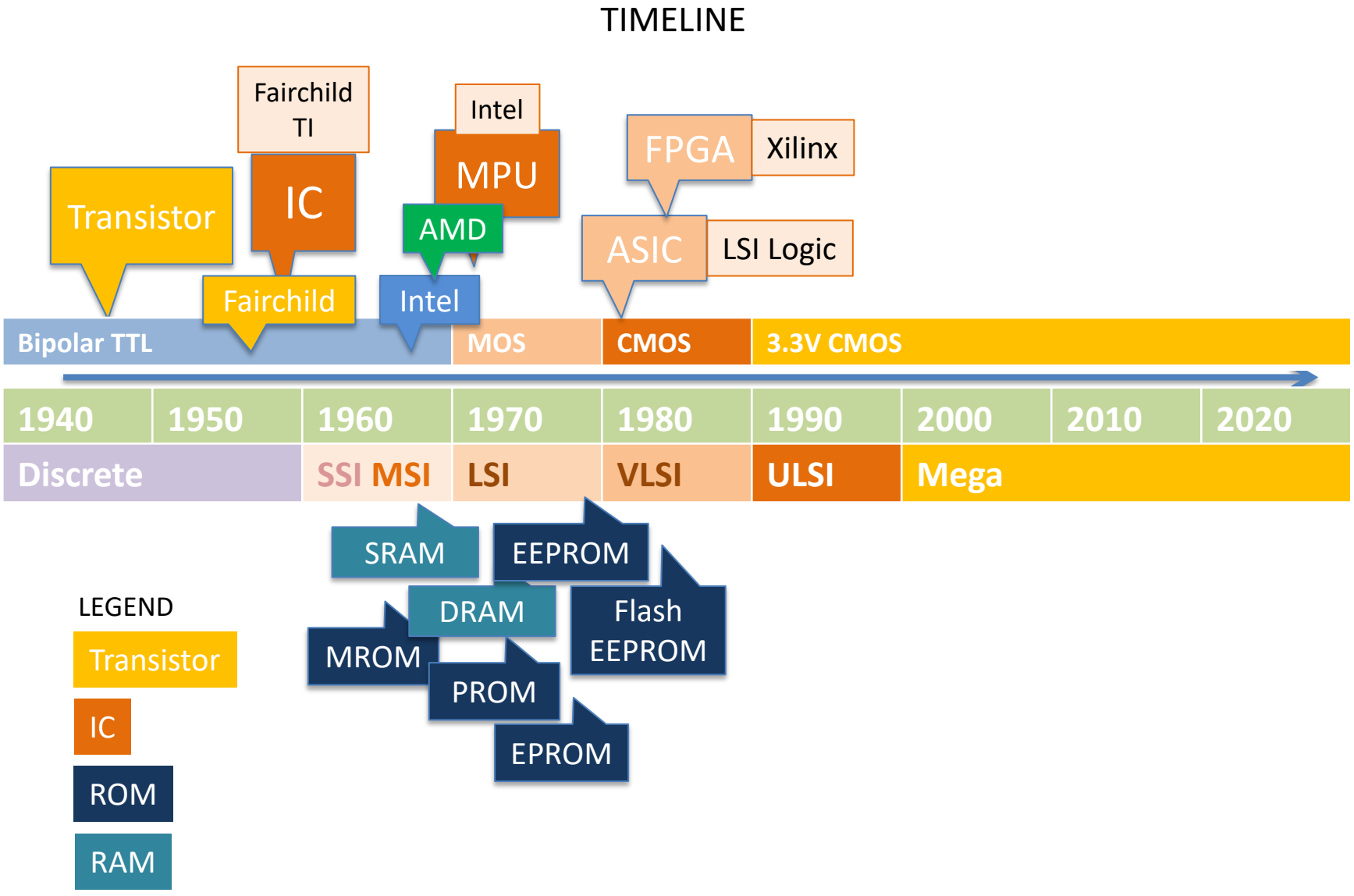

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# Section

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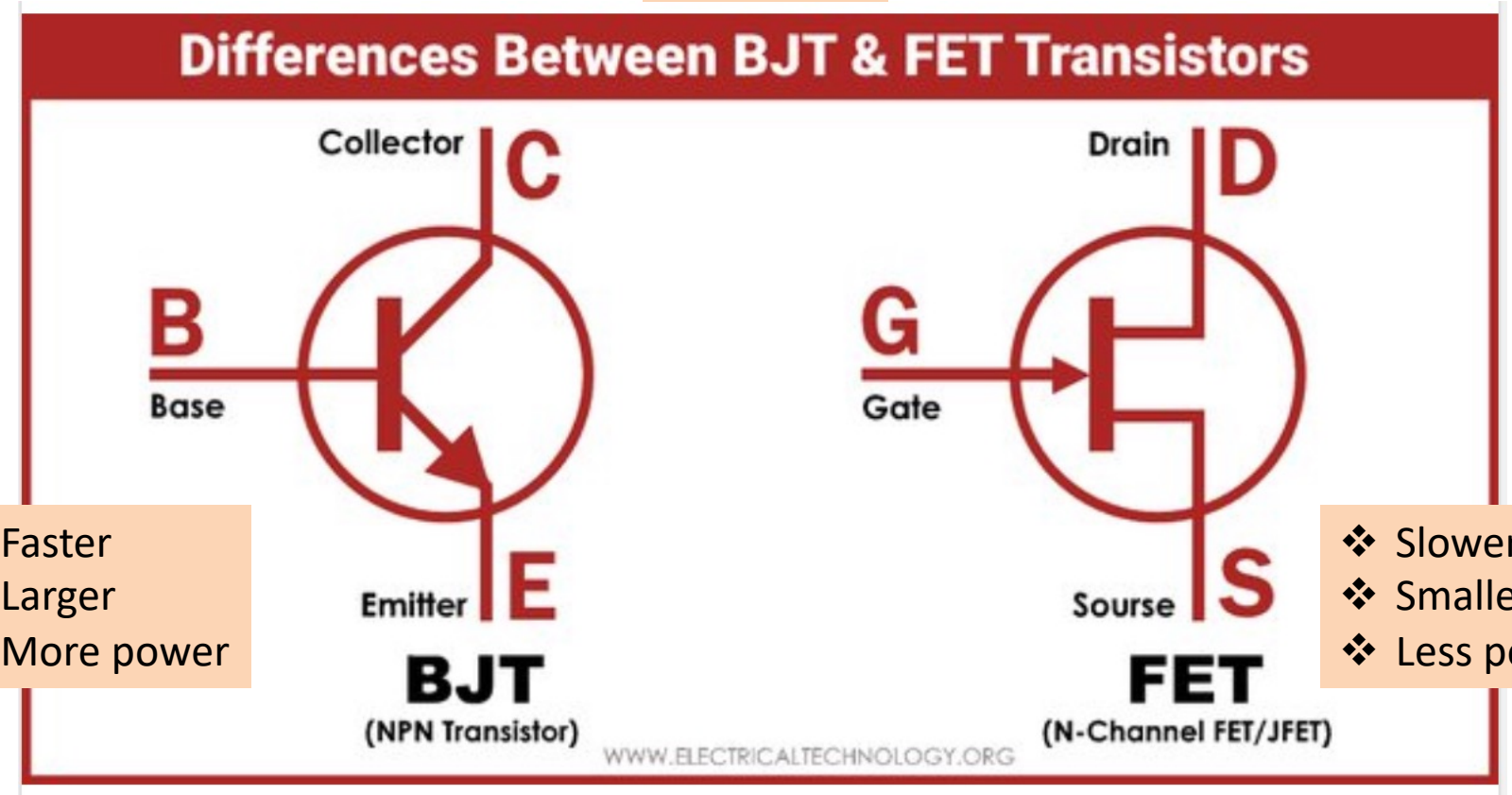
# Bipolar
# (BJT)
# Transistors

# Bipolar/MOSFET Transistors



Schematics




- Faster
- Larger
- More power

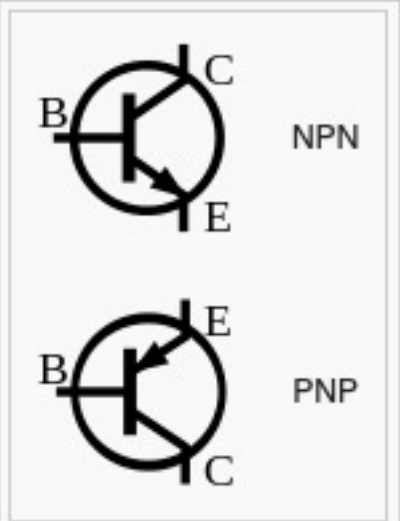
- Slower
- Smaller
- Less power

- Current flows opposite electrons (C->E, S->D)
- B, G are inputs (H/L)
- B, G voltages turn transistor ON/OFF
- Outputs (not shown) are tied to C, D

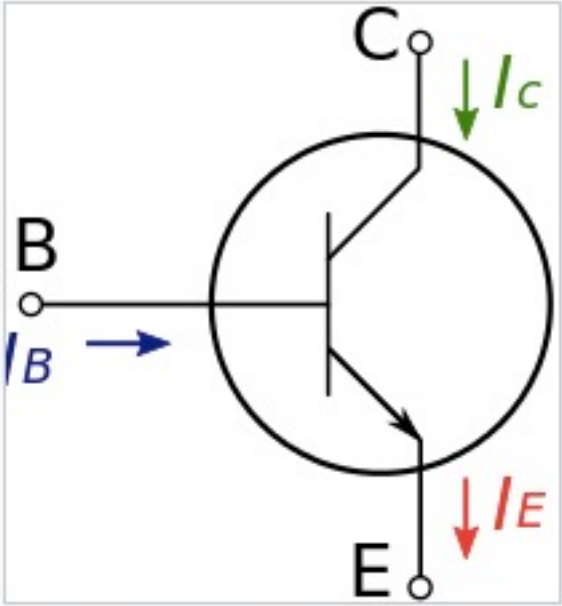
# Bipolar Transistors



## BJT




BJT schematic symbols



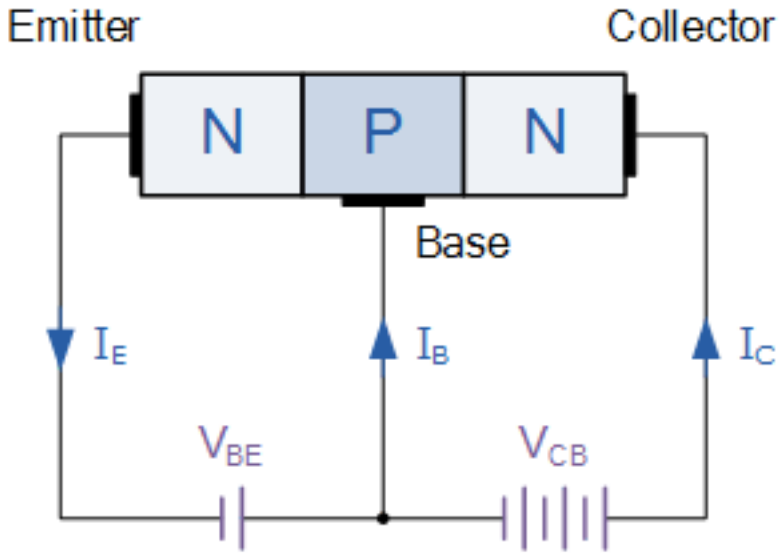

Symbol for NPN bipolar transistor with current flow direction

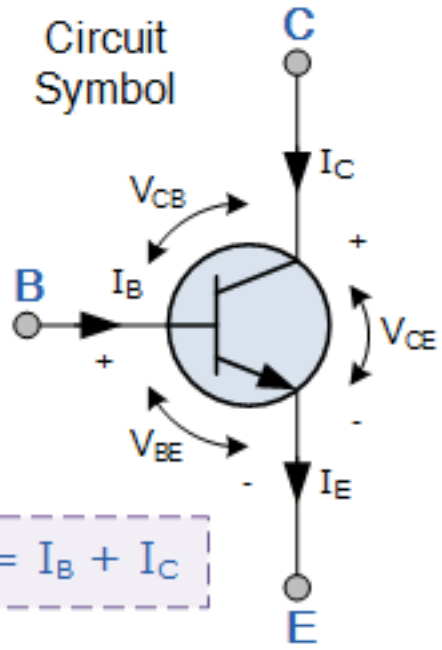

Typical individual BJT packages. From top to bottom: TO-3, TO-126, TO-92, SOT-23

# Bipolar Transistors



## BJT



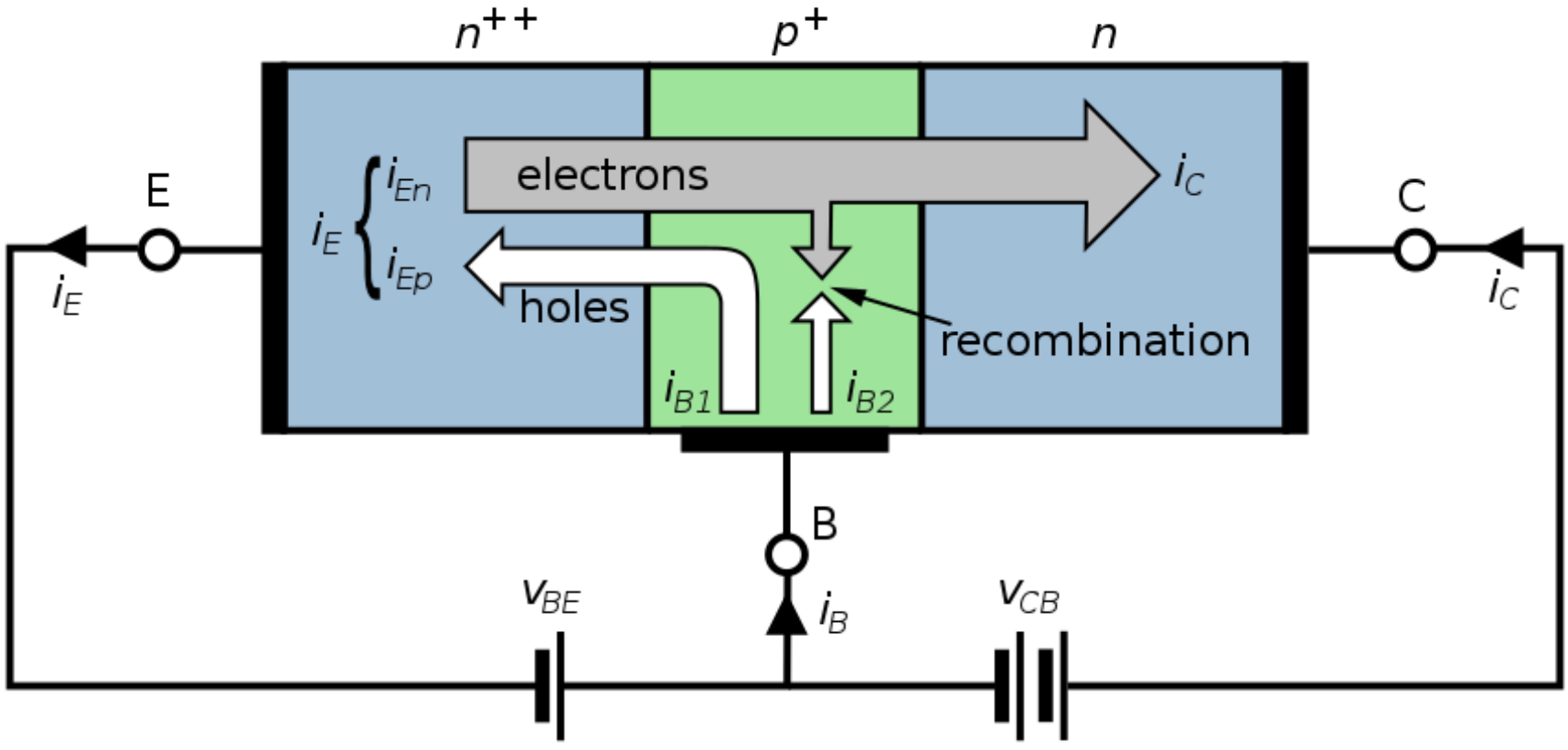




$$I_E = I_B + I_C$$

# Bipolar Transistors



## BJT

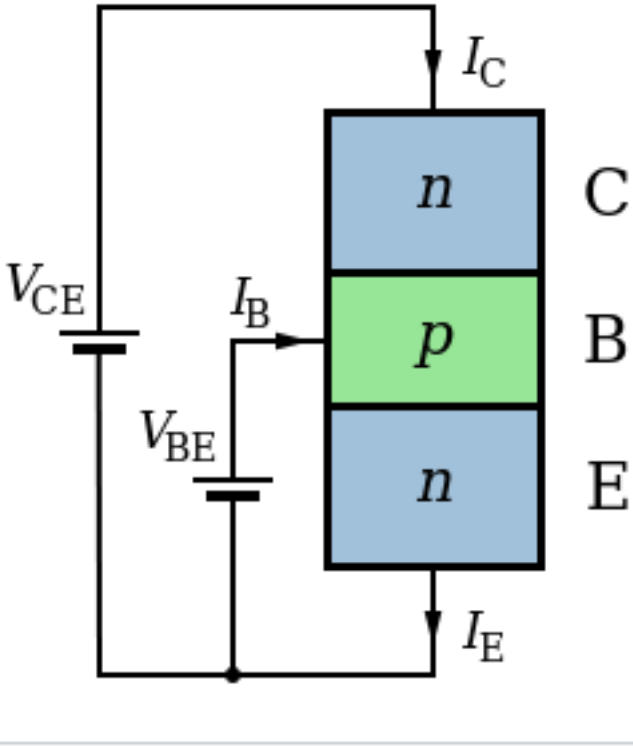



NPN BJT with forward-biased E–B junction and reverse-biased B–C junction

# Bipolar Transistors



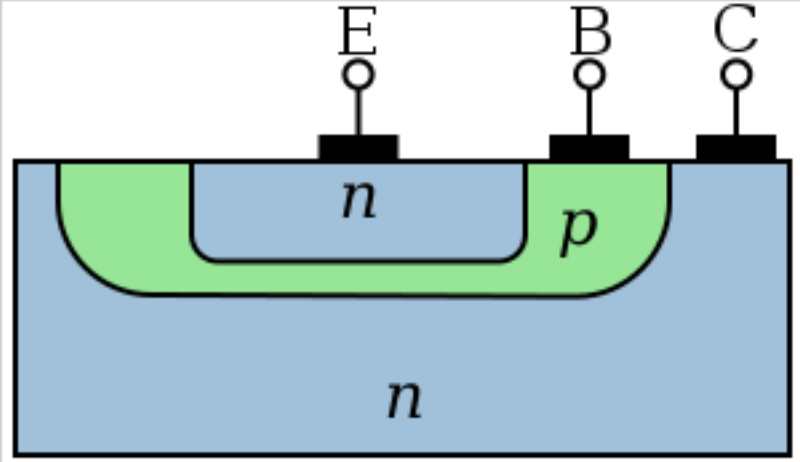
BJT




Structure and use of NPN transistor. Arrow according to schematic.

PLANAR

## Structure [edit]

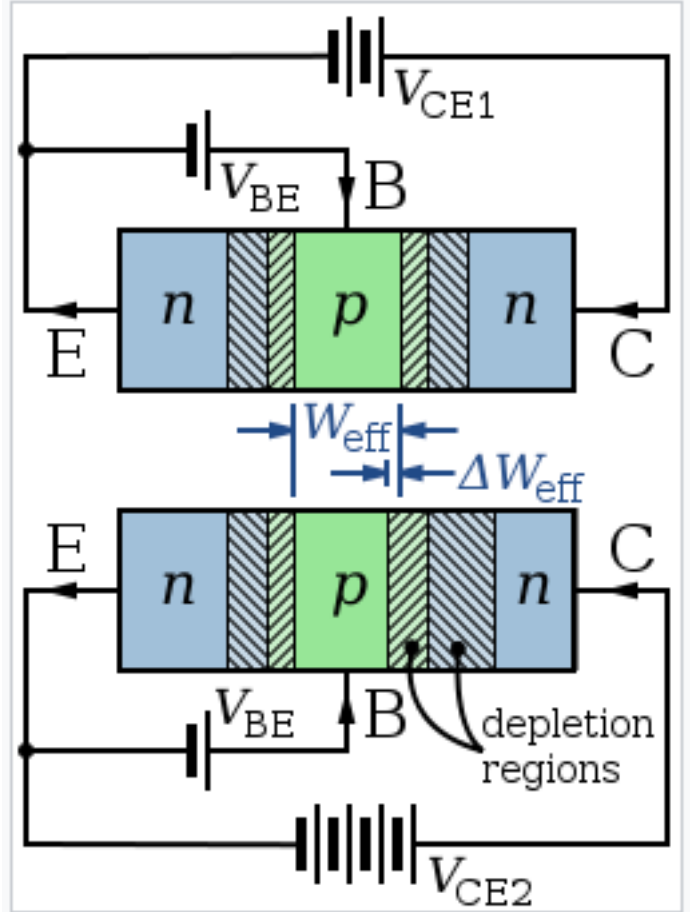



Simplified cross section of a planar *NPN* bipolar junction transistor

# Transistors




## BJT



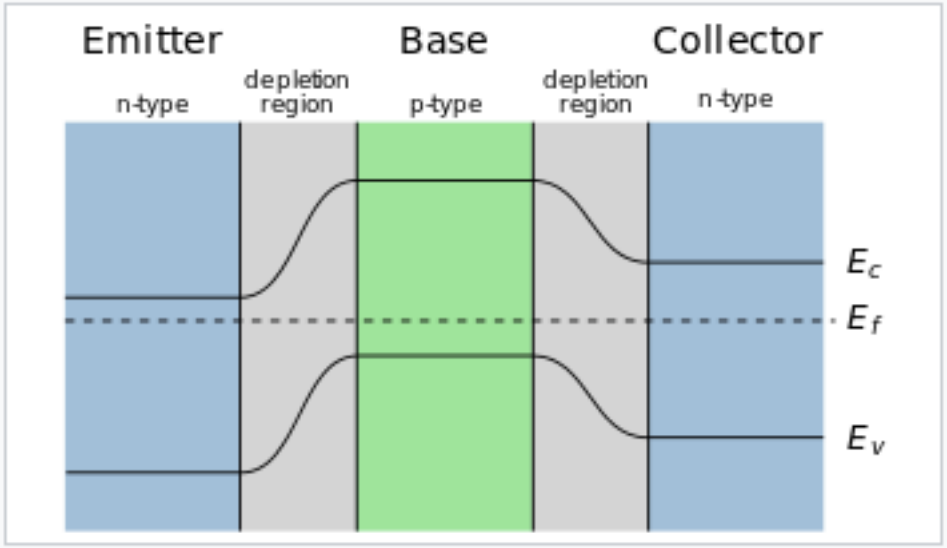

Top: NPN base width for low collector–base reverse bias; Bottom: narrower NPN base width for large collector–base reverse bias. Hashed regions are depleted regions.

Depletion Regions

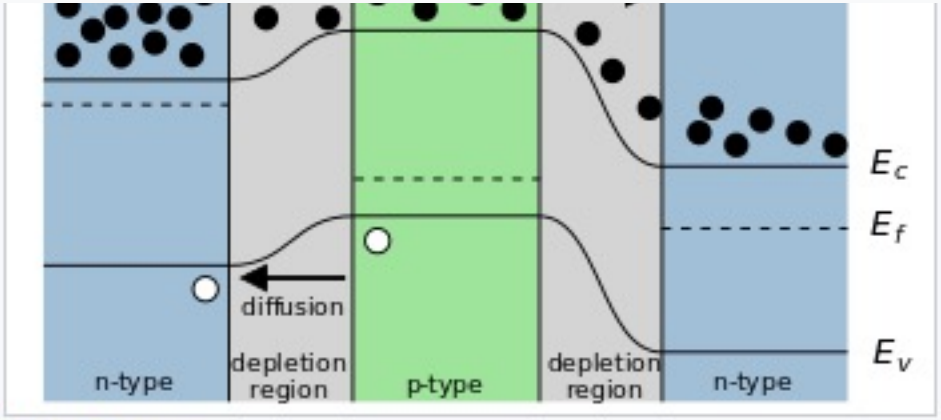
# Transistors




## BJT



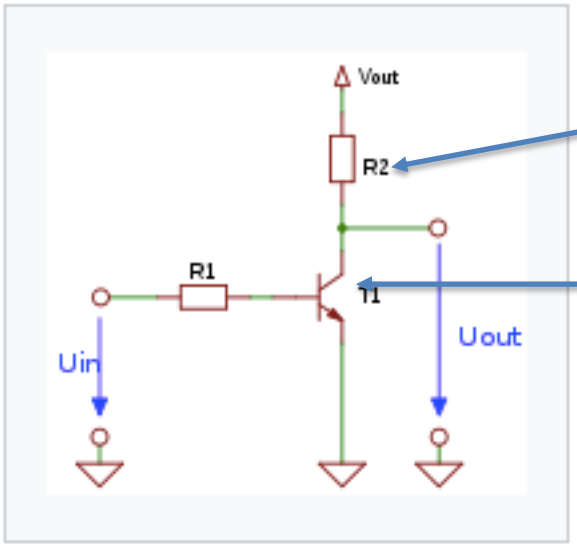

Band diagram for NPN transistor at equilibrium




Band diagram for NPN transistor in active mode, showing injection of electrons from emitter to base, and their overshoot into the collector

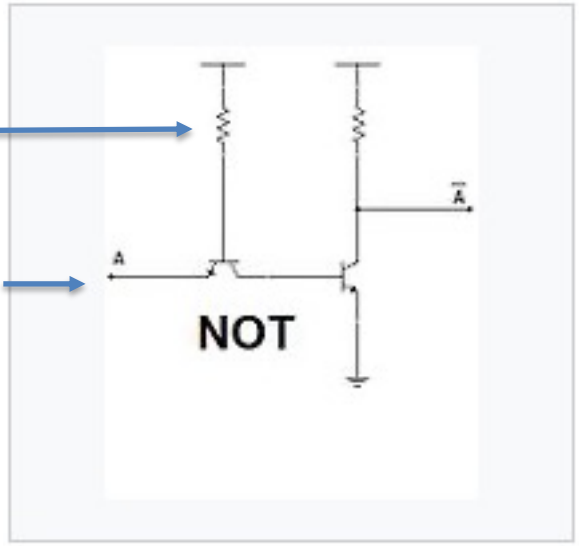
# BJT Gates






LOAD

Switch

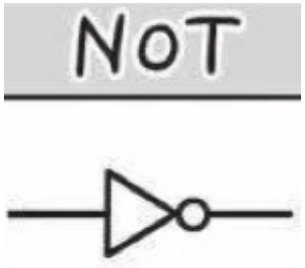



NPN resistor–transistor logic inverter

RTL

NPN transistor–transistor logic inverter

TTL



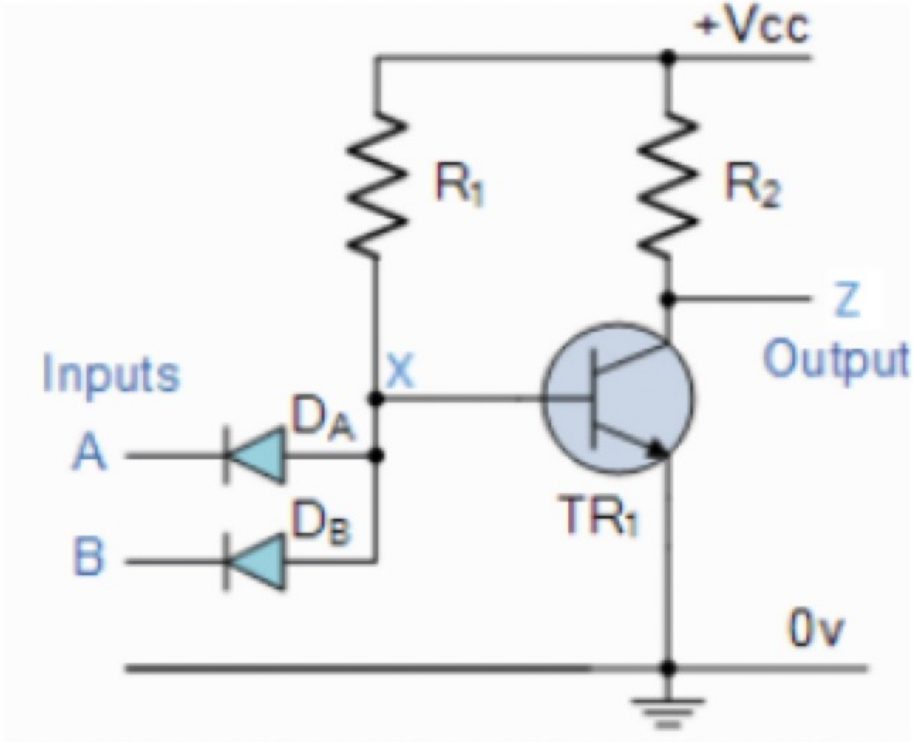
# BJT-DTL NAND Gate



Quora

1T

A DTL NAND gate is pretty easy to build using a single NPN bipolar transistor and a diode for each input:



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# BJT-TTL NAND Gate

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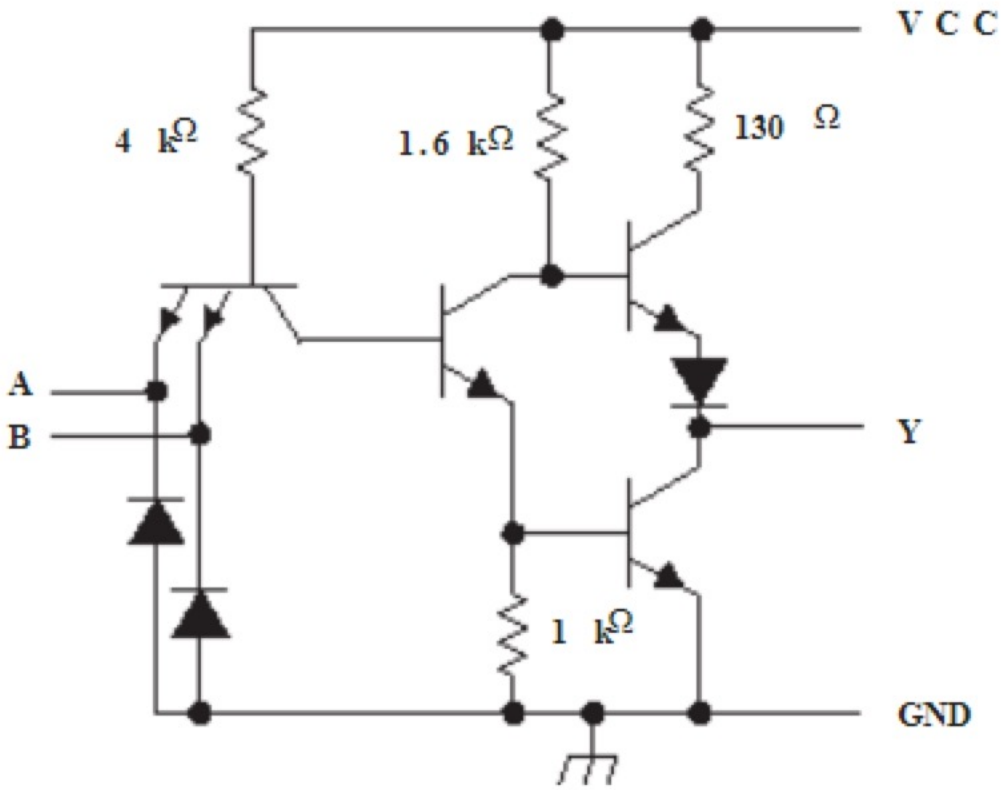
Quora

4T

Each gate in the original 7400 TTL quad 2-input NAND had four bipolar transistors, with the input having multiple emitters, one for each input with associated diodes:



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# Section

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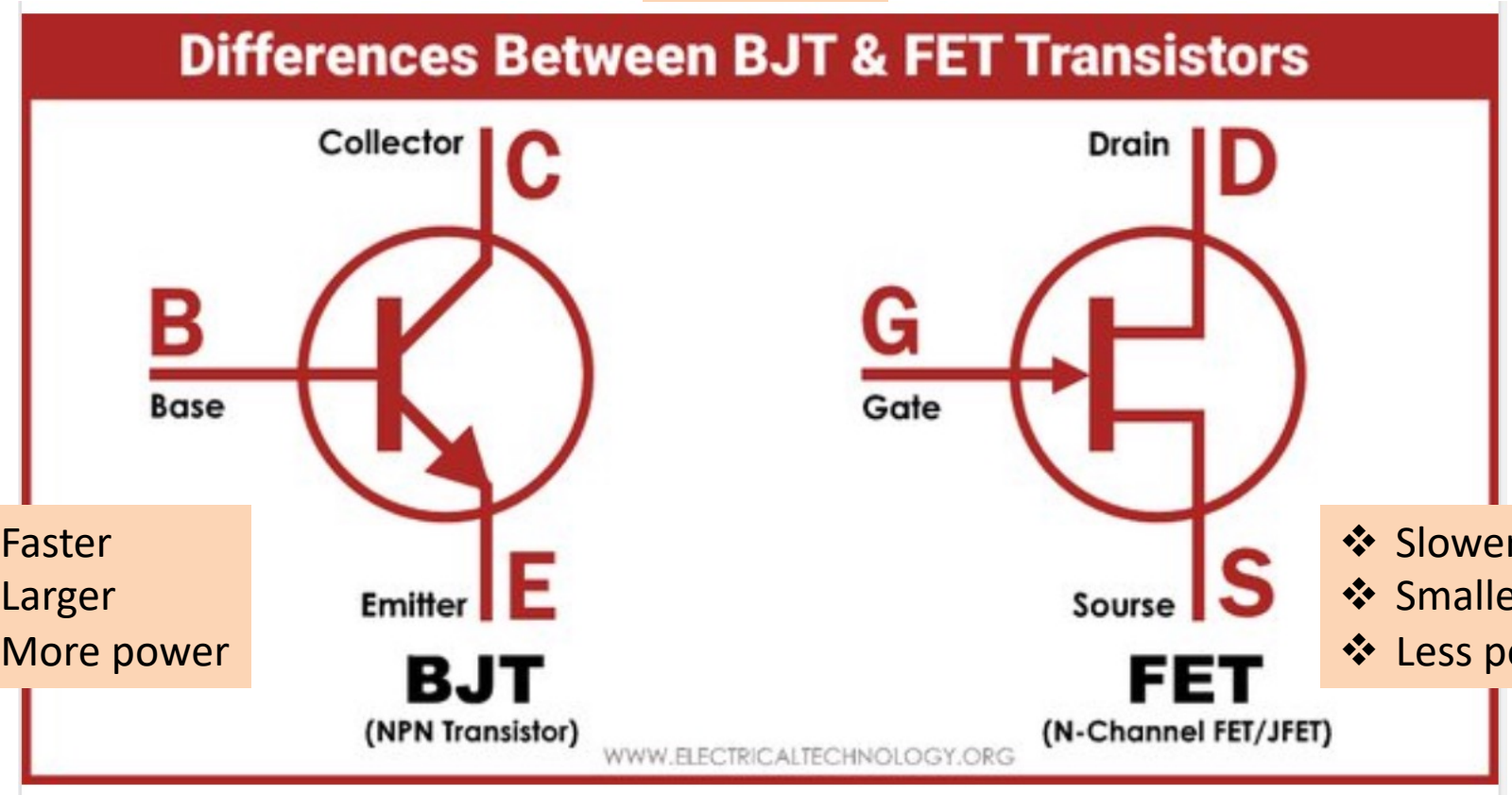
# MOS
# (FET)
# Transistors

# Bipolar/MOSFET Transistors



Schematics

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- Larger
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- Current flows opposite electrons (C->E, S->D)
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- B, G voltages turn transistor ON/OFF
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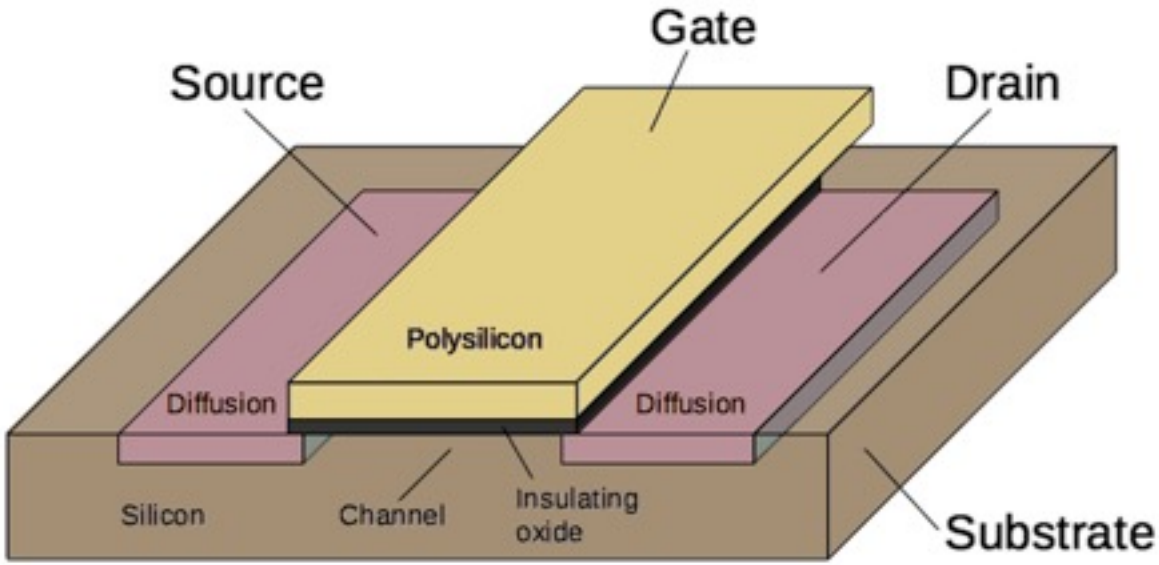
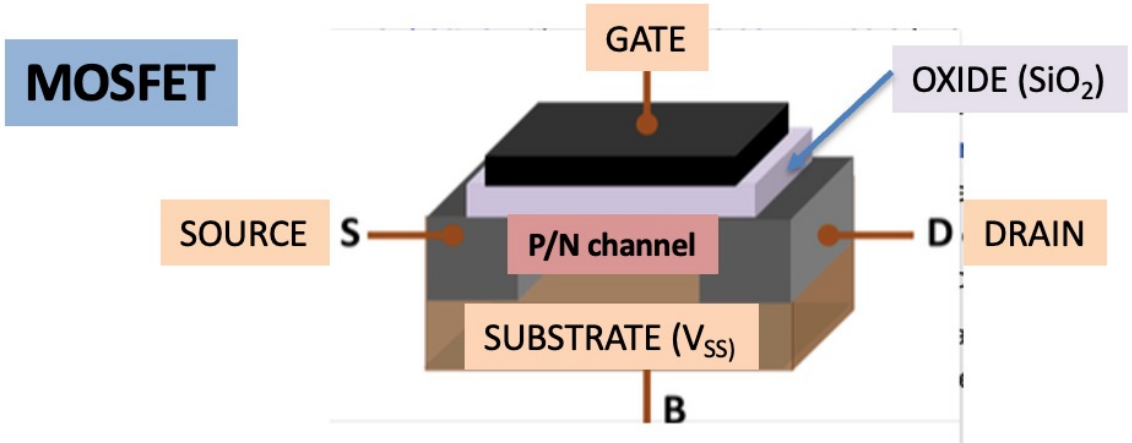
# MOS Transistor




WikiSemi




*Structure of a MOSFET in the integrated circuit.*



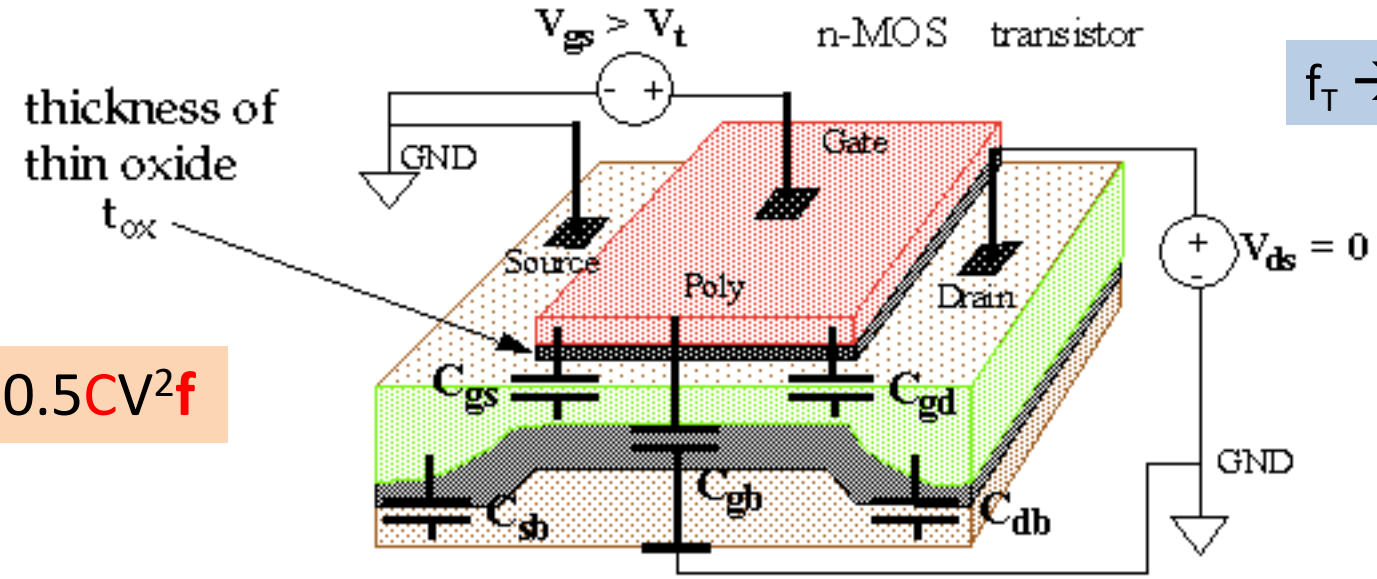
# MOS Transistors



The channel will have a length (distance from one electrode to the other) and a width (imagine this diagram coming out of the screen). The electrodes have geometries. The gate doesn't always span the full width of the channel and is its own critical dimension.

The sizes of each of these things are critical dimensions. They all have an effect on the performance of the device because they will contribute parasitic capacitance and resistance.

Parasitic capacitances




$f_T \rightarrow$ lengths

$P = 0.5CV^2f$

*Parasitics depicted by University of New Mexico*

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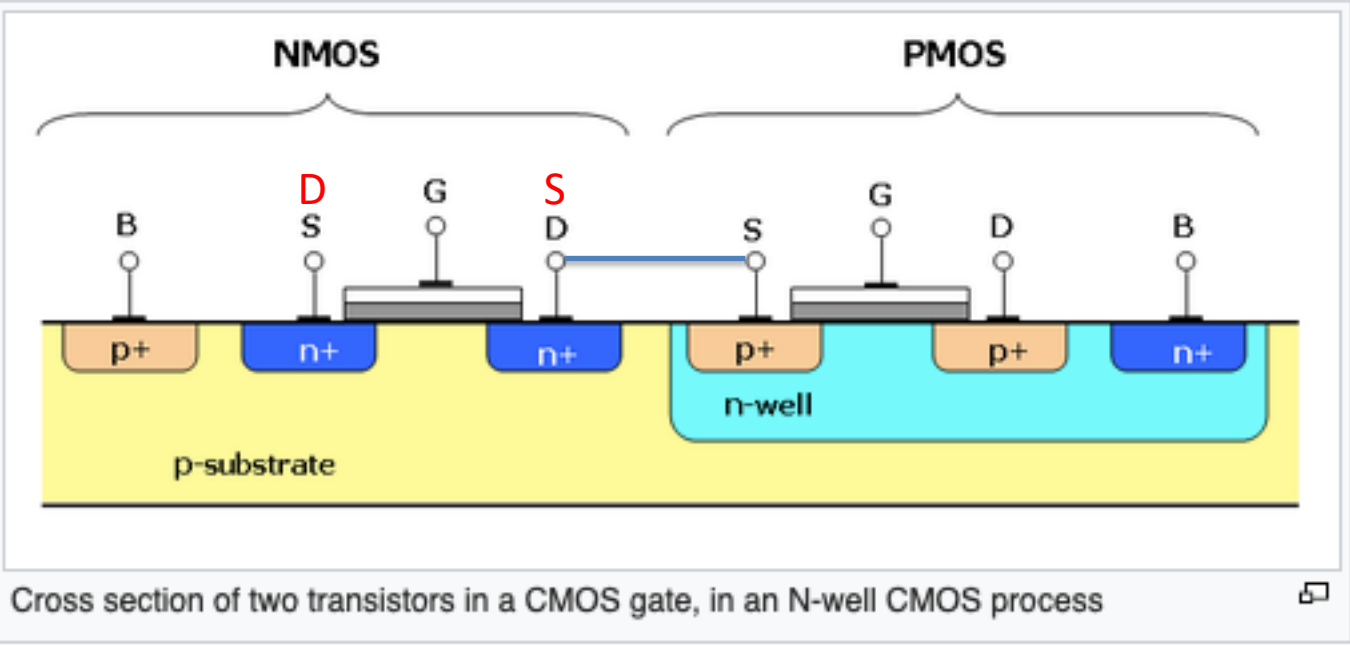
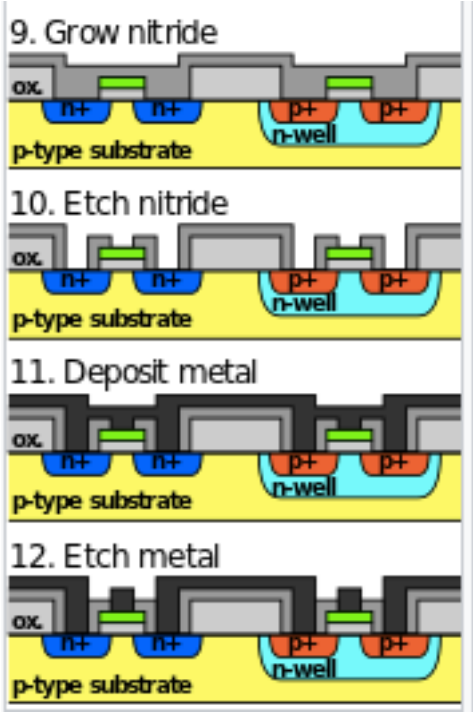
# CMOS Transistors

## MOSFET




Cross section of two transistors in a CMOS gate, in an N-well CMOS process

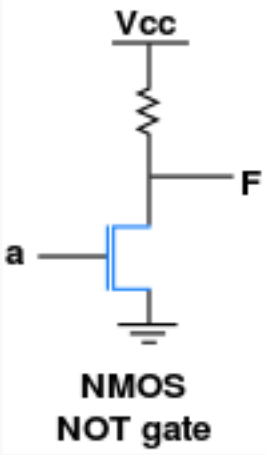



Last 4 steps

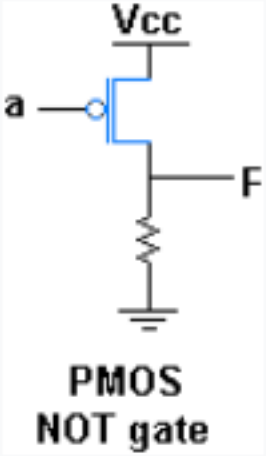
# MOS Gates



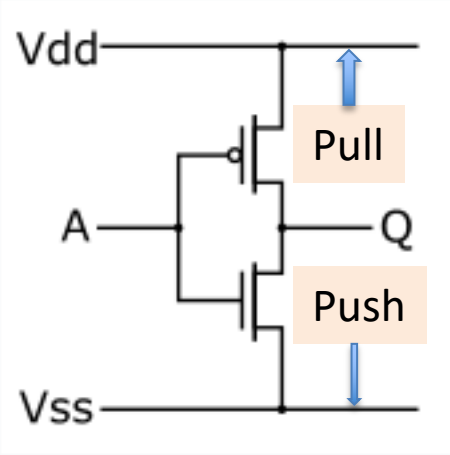
## MOSFET



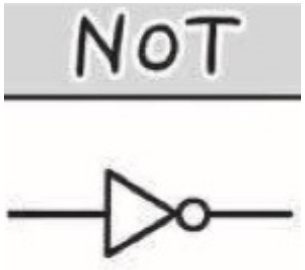

NMOS inverter




PMOS inverter




Static CMOS inverter




CMOS

P/N Totem pole

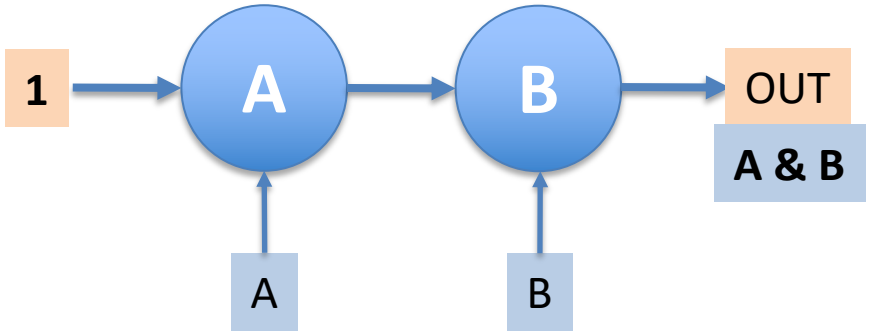
Push-Pull

# Logic Gates: AND, OR



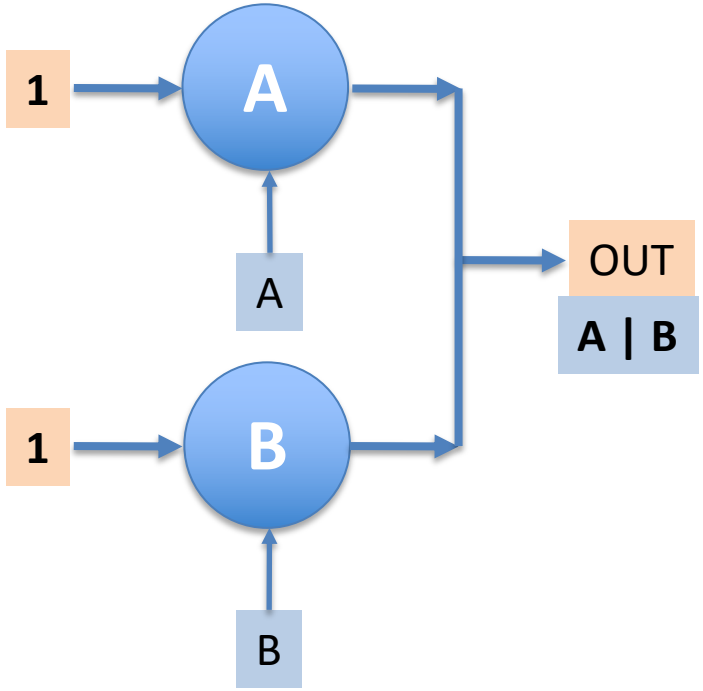
## AND

SERIES




## OR

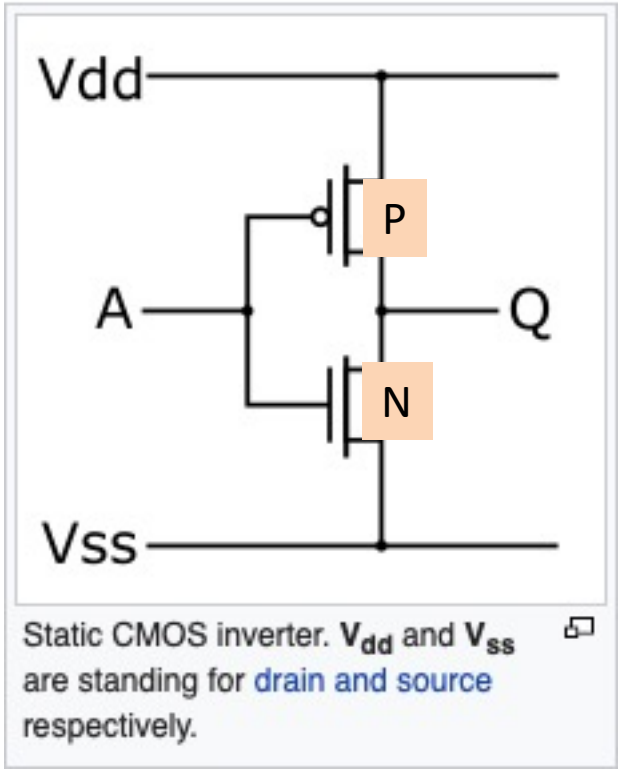
PARALLEL



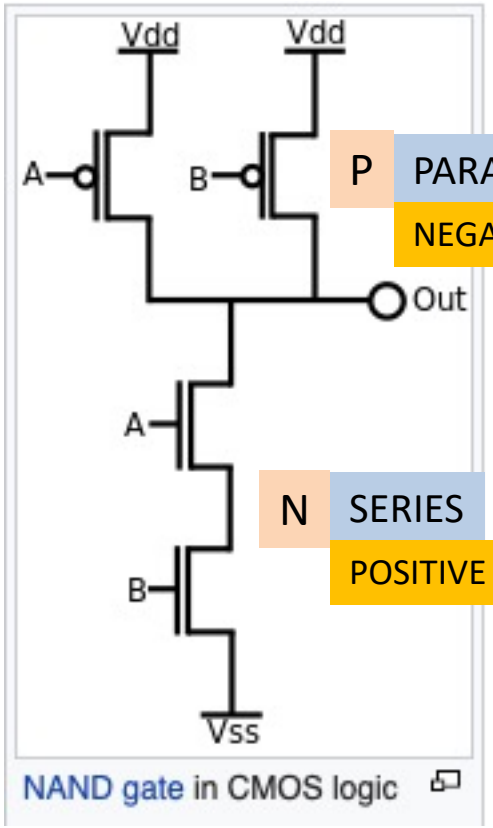
# CMOS Gates



## MOSFET



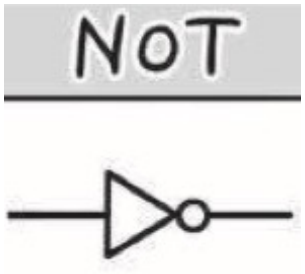

Static CMOS inverter. $V_{dd}$ and $V_{ss}$ are standing for drain and source respectively.

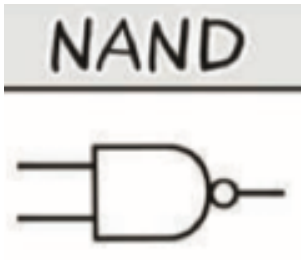



NAND gate in CMOS logic

P PARALLEL
NEGATIVE OR

N SERIES
POSITIVE AND



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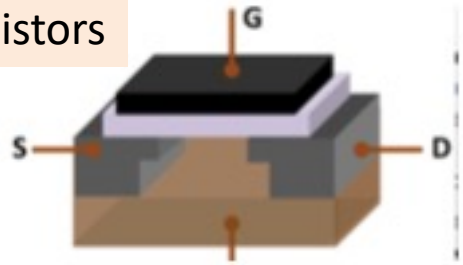
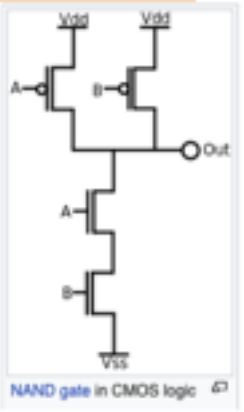
# 3 Levels of Integration

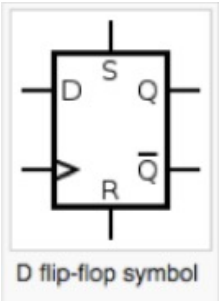
## Hardware Building Blocks

### 0- Transistors

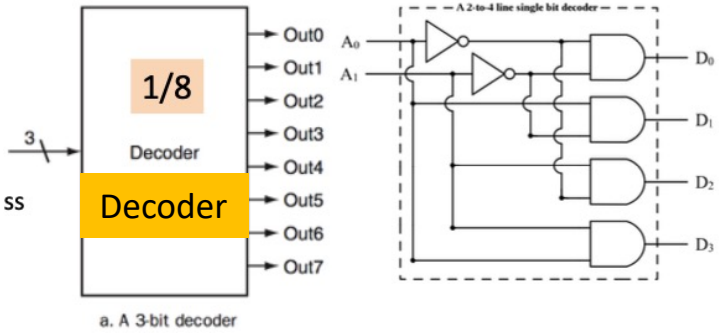


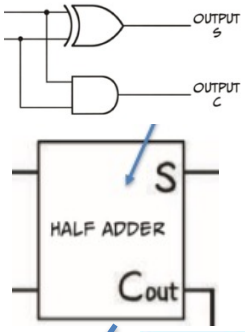

### 1- Gates & FF's

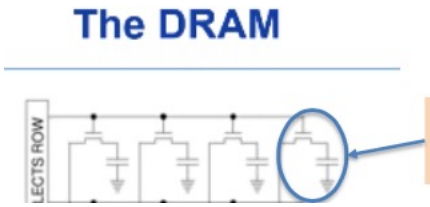




### 2-Single Functions



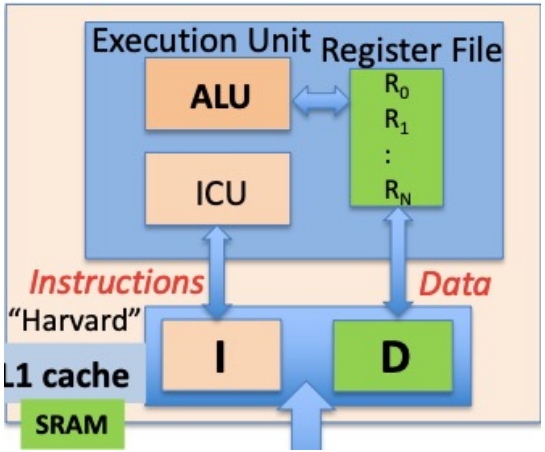




### Memory Cells

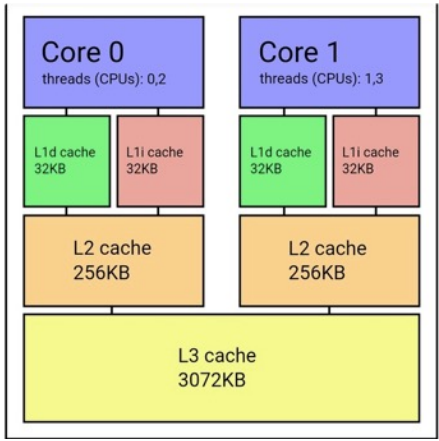


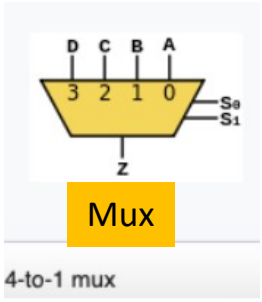

- 1 transistor
- 1 cap (parasitic)

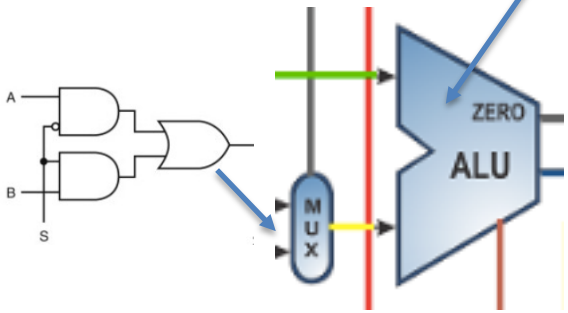
### 3-CPU




### 3-Multi-core CPU

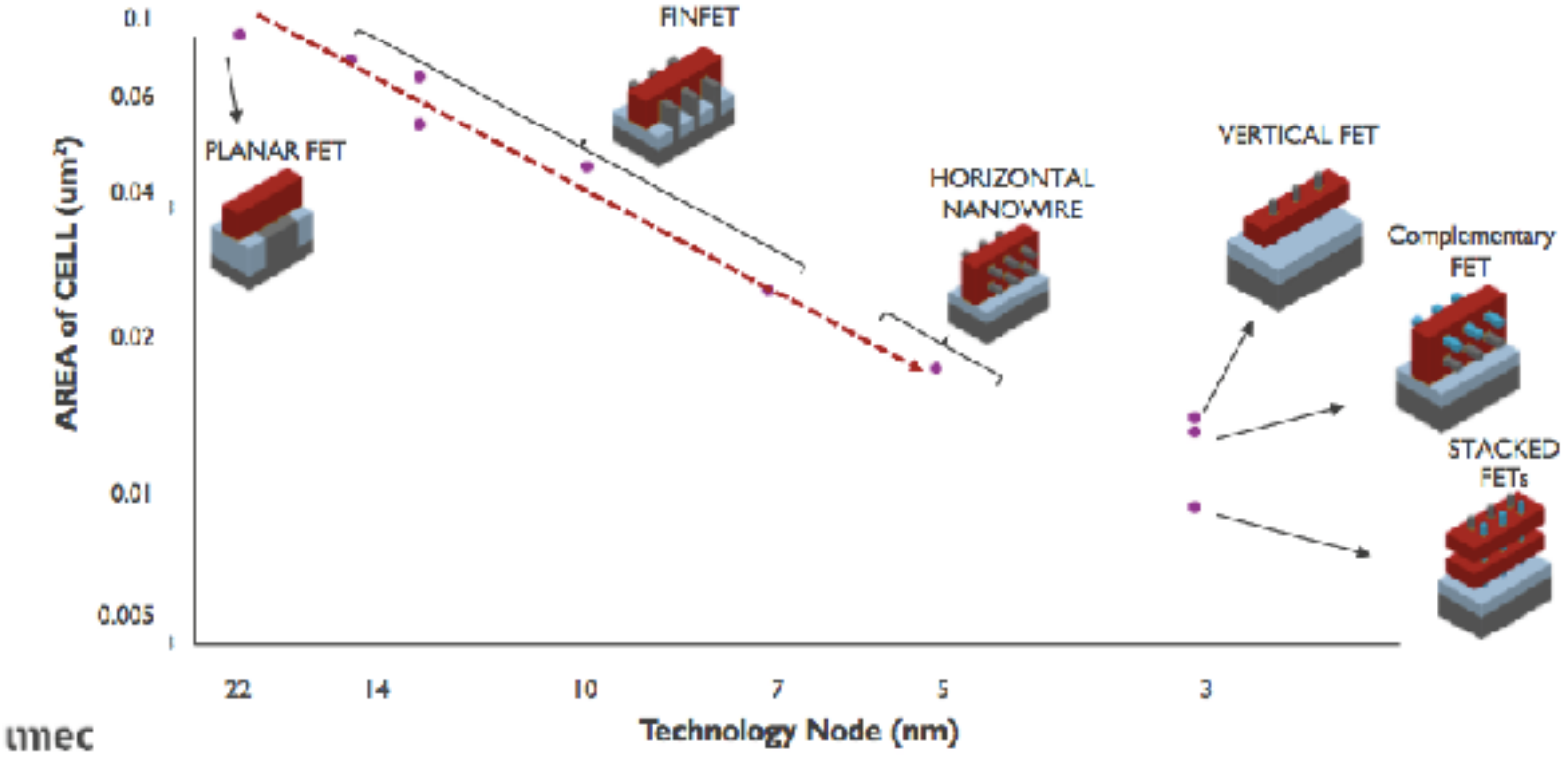


# Transistor Processes



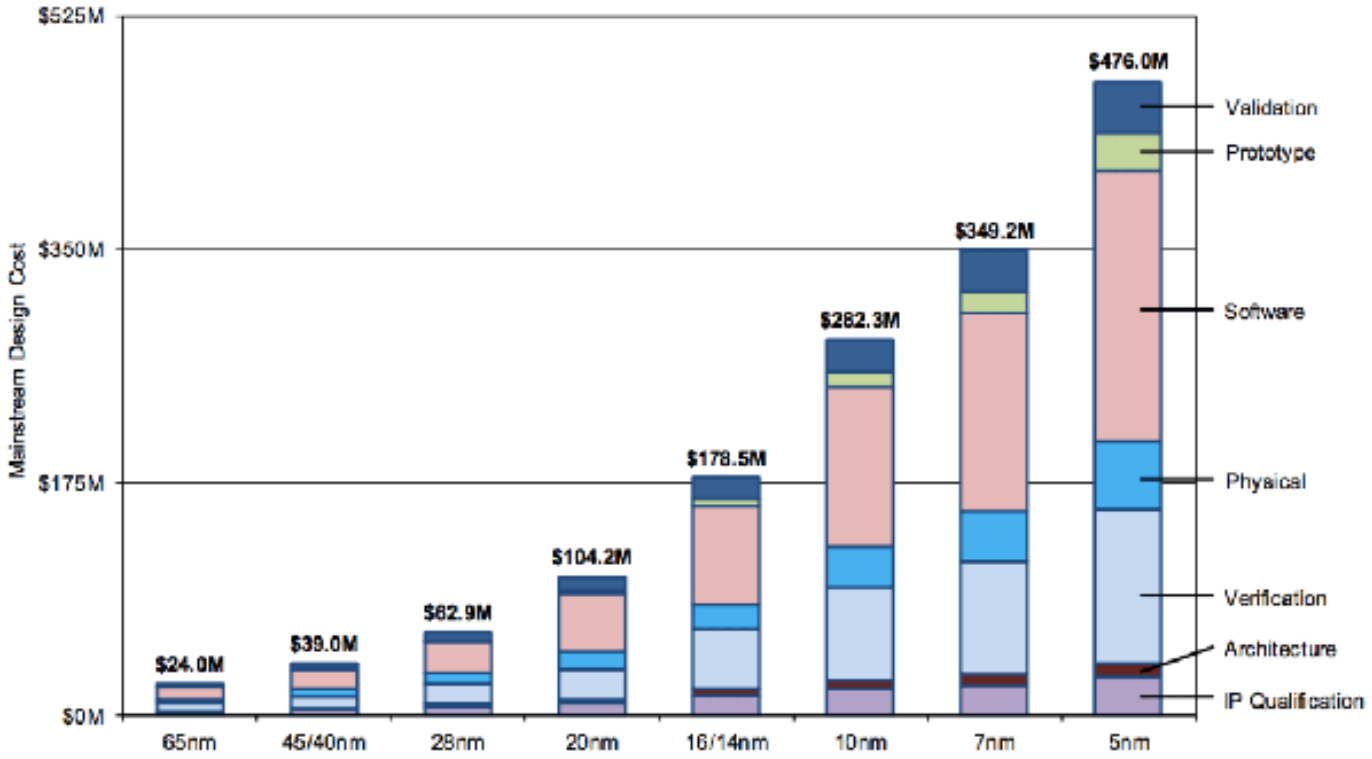



Moore's Law →

# Transistor Processes



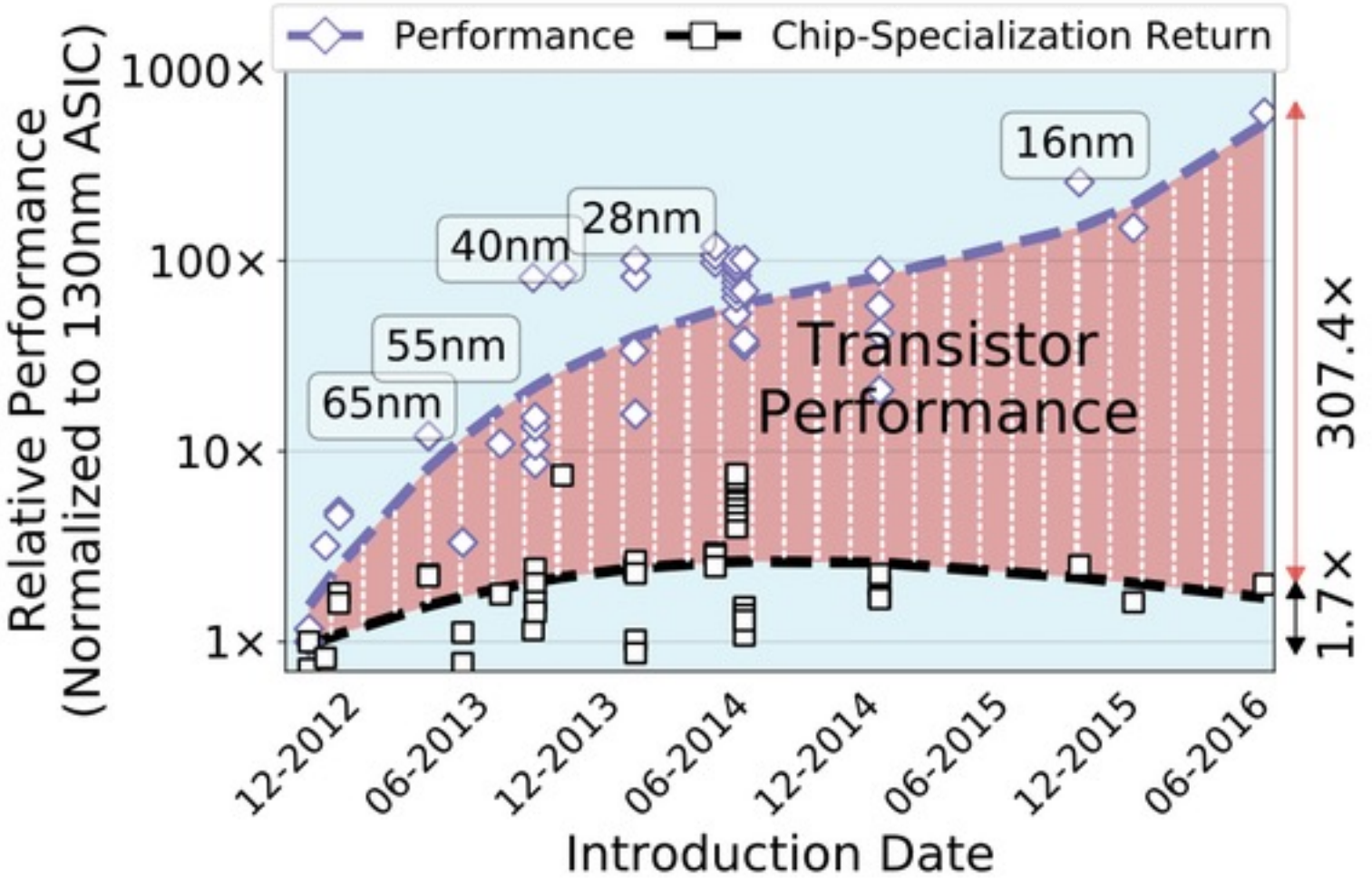
In the short run, there is nothing stopped chips from adopting 'smaller' nodes (3–1 nm) but by 2023–2025, the cost of development, equipment, tooling will become so high and FinFET scaling will plateau, meaning that alternative post-FinFET devices will have to developed to ensure that performance continues to scale.




There are multiple concepts such as gate all around FETs (GAA-FETs) and FETs with horizonal nanowire being explored but none are currently viable for high volume IC.

# Chip Specializations






*On-chip specialization or microarchitctural changes merely account for a fraction of the performance gains.*

# Chip Fab: FinFET



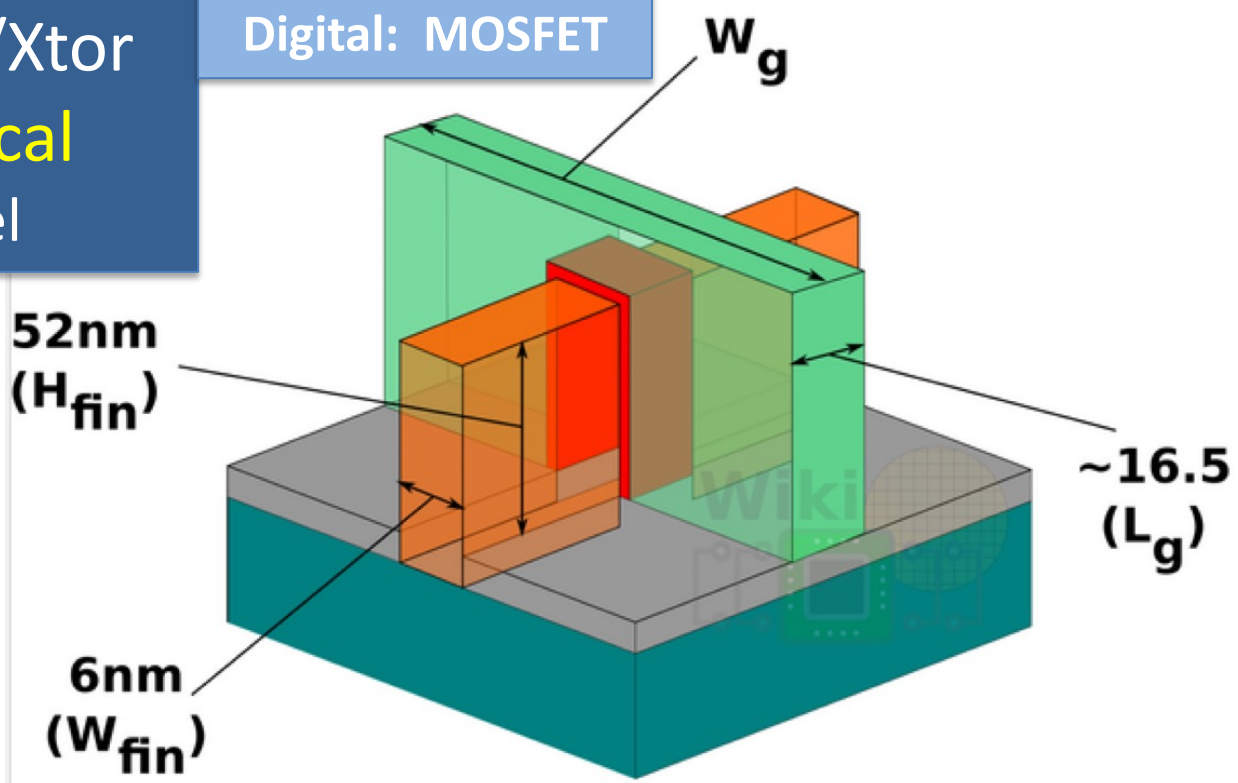

7 nm **TSMC**

Device/Xtor
Physical
Level

**Digital: MOSFET**

What's a 5nm FinFET transistor look like?

Well... I didn't find a good pic for 5nm, but I found a pic for 7nm here:




We can assume 5nm is slightly smaller on all axes.

The first thing to note is that the gate length ($L_g$) is 16.5nm. The width of the gate will vary, but I am going to go out on a limb and guess it is no smaller than $3W_{\text{fin}}$, or 18nm. And the overall structure is tall: 52nm plus another few nm

CSUN
CALIFORNIA STATE UNIVERSITY NORTHRIDGE

# MOSFET Evolution

DR JEFF SOFTWARE
INDIE APP DEVELOPER

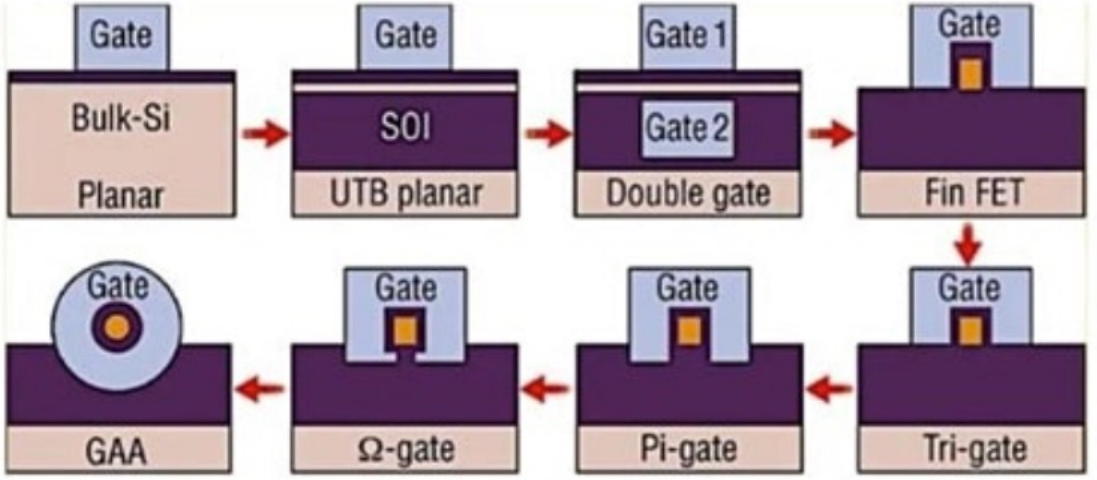

Device/Xtor
Physical
Level

**Digital: MOSFET**

IEEE

## Nanoscale FinFET Technology for Circuit Designers

Alvin L.S. Loke, NXP



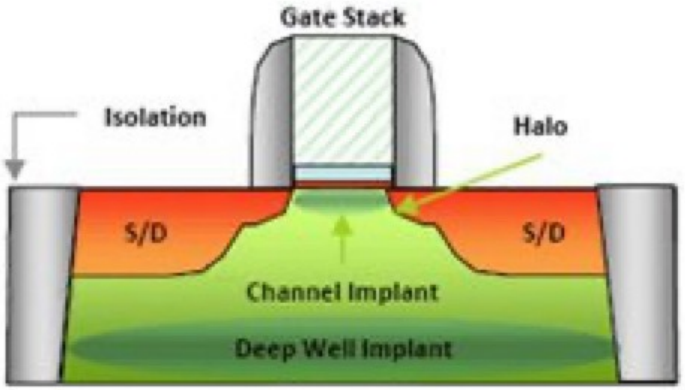
# 3nm FinFET



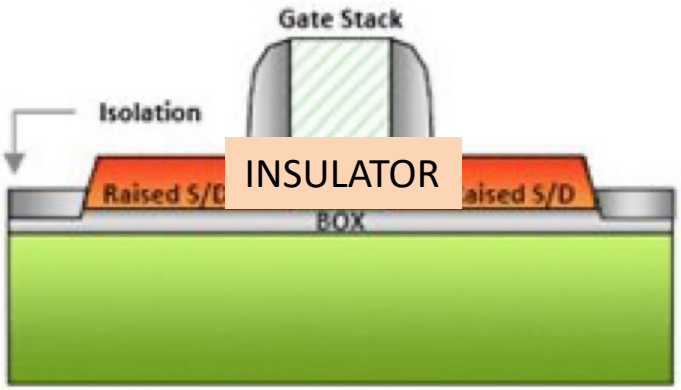
SOI

**Digital: MOSFET**

Another possibility is to move back to Silicon on Insulator (SOI) with a modified FD-SOI MOSFET. These would use a channel made of something other than monocrystalline Silicon with the intention of engineering for a more constrained electron wave-function. [Sorry, it truly is impossible to talk modern semiconductors without invoking Quantum Mechanics at some point]




Bulk Device

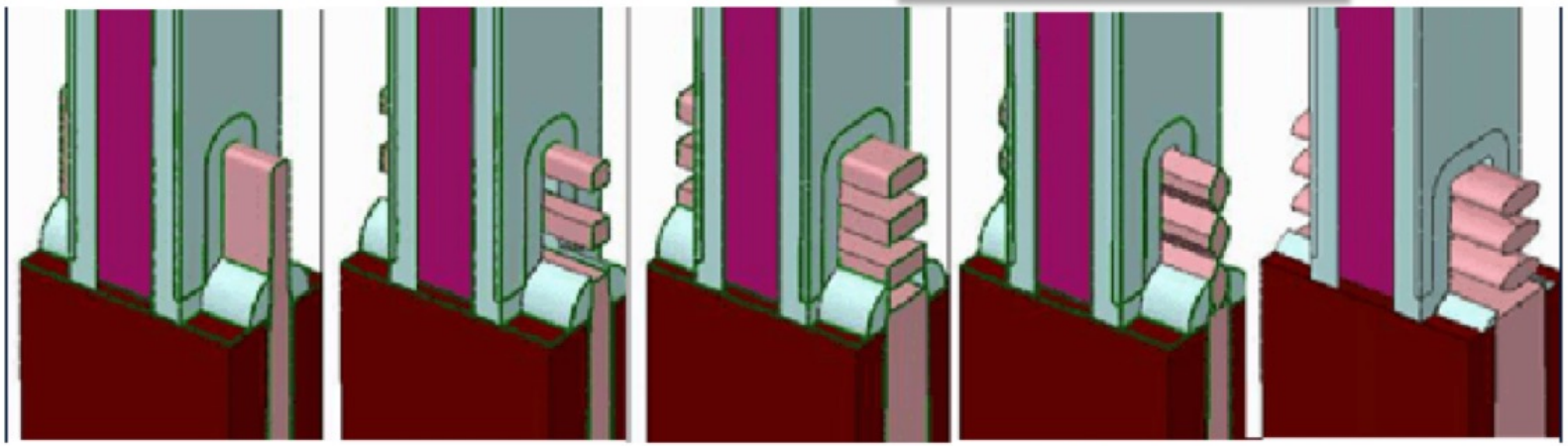



FD-SOI Device

# 3nm FinFET




**Digital: MOSFET**



Ref: S.C. Song, Qualcomm; V. Moroz, Synopsys

| Traditional FinFET | Round/Square Wire | Horizontal Nanoslab/sheet/ multi-bridge channel | Hexagonal Nanowire | Nano-Ring |
|---|---|---|---|---|
| Three control surfaces | Four/All Around Control Surfaces Per Channel | | | |

All around gates were believed essential to 7nm and beyond but 7nm was developed just fine on FinFETs and TSMC has demonstrated 3nm FinFET manufacturing as of 2020. Unfortunately, no “need” translates to limited development in HVM environments.